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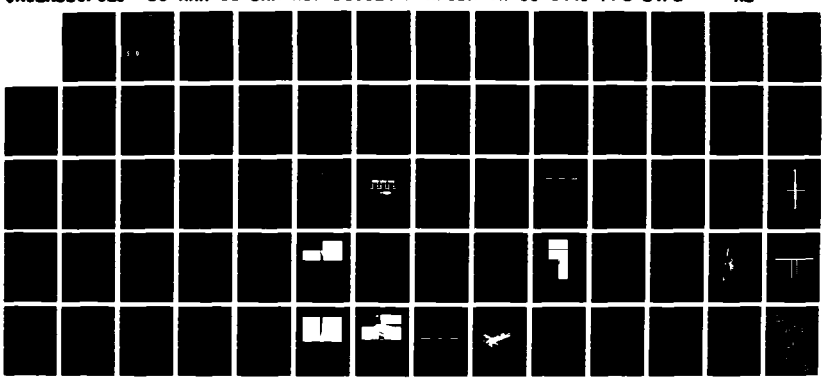

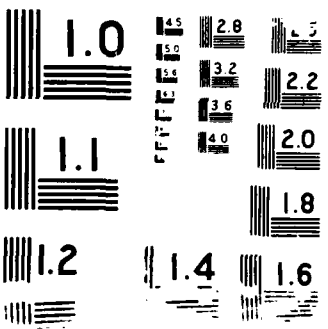
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NUMERICAL SIMULATION OF THE FUNCTION OF SCIENTIFIC INSTRUMENTATION FOR MEASURING THE SPEED OF ELECTRON DEVICES

Prepared by

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for

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The feasibility of using numerical simulation to asses the function of scientific instrumentation for measuring the speed of electron devices has been demonstrated by obtaining (1) the dc characteristics of the VHEMT and PHEMT, (2) transient response of the PHEMT to picosecond voltage pulses superimposed on the gate. The drift and diffusion and Poission's equations were solved in two dimensions. The VHEMT and PHEMT demonstrated transconductance of 94 and 375 mS/mm, respectively. The transient response is strongly dependent on the pulse shape and duration.

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1. INTRODUCTION

The development of techniques to generate laser pulses with picosecond and sub-picosecond duration has finally provided the means to probe ultrafast relaxation processes in semiconductors and to determine the response time of new high speed devices. Mourou and his group have used picosecond electro-optic sampling techniques to characterize such ultrafast transistors as the High Mobility Electron Transistor (HEMT), Permeable Base Transistor (PBT) and GaAs MESFET [1,2]. They measured a 10%-90% rise time of 16 ps for the HEMT, and 5.3 ps for the PBT. Figures 1 and 2 show the sampling geometry used for characterizing the HEMT and PBT, respectively. Similarly, Nuss and Austin [3], using electro-optic sampling techniques examined the picosecond transient mobility of electrons in GaAs. The electroptic sampling technique is new. It provides high temporal resolution, ranging from 100 → 300 femtoseconds, and is likely to improve as our combined understanding of the electroptic effect, the photoconducting effect, and ultrafast relaxation processes improves. The improved temporal resolution is necessary for measuring the response of the new emerging class of high speed devices such as the pseudomorphic HEMT (PHEMT) and resonant tunneling devices, as well as for testing new device concepts such as the vertical HEMT (VHEMT). The central objective of this Phase I SBIR was to assess the function of scientific instrumentation for measuring the speed of electron devices using numerical simulation. Fulfilling this objective requires:

(1) a thorough understanding of the characteristics of those devices chosen for study, and

(2) a thorough understanding of the signature of the instrumentation used for measurement.

For example in the case of the electroptic sampling technique of Mourou, the signature is the shape of the pulse, its duration, rise time, and its dependence on those material parameters that control it, such as the recombination processes in the photoconductor. While all aspects of this could not be studied during the Phase I, key elements were examined. These included:

(1) characterizing two devices, the PHEMT and VHEMT, through numerical simulation, and,

(2) examining the transient response of one of these devices, the PHEMT, to picosecond pulses with different shapes and rise times. This output of the study closely resembles the electroptic sampling approach, except for the details of how the photoconductor shapes the electrical pulse that perturbs the gate bias, and how the probe beam samples the electroptic material.

The two structures chosen for study are summarized below.

1.1 Vertical HEMT:

The vertical HEMT was proposed by the same group that developed the PBT at Lincoln Laboratory[4], and represents an evolution in vertical transistor design that incorporates many of the favorable features of both the PBT and

HEMTs and avoids some of the surface state problems affecting many other vertical FET configurations. For example, while measurements indicate that the PBT is currently the three-terminal device with the shortest response ever recorded, efforts to achieve satisfactory microwave and millimeter require techniques to reduce the emitter-base capacitance. The first attempt to introduce design changes was proposed by Osman et al [5] who demonstrated through numerical simulation studies that a dielectric with a low surface charge density at the dielectric/GaAs interface could significantly reduce the base-emitter capacitance. Unfortunately, most available dielectrics suffer from the inherent Fermi level pinning at the interface, creating a depletion region that extends from the gate to the source, and rather than improving, further degrades the performance of the PBT [5]. Although introducing a highly doped layer near the surface could reduce the effect of Fermi level pinning, such an approach reduces the mobility of electrons as a result of impurity scattering and increases the capacitance of the device. In the case of the VHEMT, an alternative approach, through modulation doping technology. is used to reduce the parasitic capacitance. For the VHEMT, as shown in figure 3, (1) the gate does not penetrate the conducting channel, as in the PBT, and (2) a very high doped AlGaAs layer is introduced to drastically reduce the effect of Fermi level pinning while maintaining a high density electrons with very high mobilities. The proposed VHEMT was anticipated to show two modes of operation:

(1) FET-like mode when the AlGaAs layer and the channel are pinched off (i.e. for reverse gate bias). The current flow is dominated by electron transport through the central channel as shown by the arrow in figure 3-a.

(2) HEMT-like mode where the current is dominated by the electron transport in 2D channel and the adjacent highly doped AlGaAs layer.

To achieve these two modes of operation careful design procedures are required, particularly with respect to the width of the conducting channel. For a combined HEMT and FET-like operation, channel widths of a few hundred angstroms may be necessary. Insofar as initial fabrication efforts are not likely to achieve this scale, wider channel widths were considered, such as that identified in figure 3. These wider channel widths introduce their own peculiarities, such as the possibility of injected charge and a degradation in the forward conductance. To overcome these difficulties a moderately doped island was introduced, as shown in figure 3b. This structure was proposed by Dr. Hollis from Lincoln Labs [6], and it was this structure that was simulated.

During the Phase I study of the VHEMT, only the operational physics of the device was studied. And it was determined that the unique concept of the VHEMT and the realization of its anticipated high current and high power capabilities require a careful approach in designing an optimum device

structure. The Phase I study indicates that the following issues need to be addressed:

(1) What is the optimum doping profile between the drain and horizontal AlGaAs/GaAs interface? For the horizontal interface, the doping levels in the GaAs layer should be adjusted to minimize electron confinement near the interface and increase the electric force on the electrons that attracts them to the drain.

(2) What is the effect thickness of the central channel region on the output current?

(3) How will the separation between the gate and the source (drain) affect the characteristics?

(4) How will the VHEMT characteristics such as the breakdown voltage change if the source and drain contacts were interchanged?

(5) What is the optimum doping level in the AlGaAs layer to achieve high current levels and transconductance?

1.2 Pseudomorphic HEMT

The enhanced electron mobility and carrier confinement afforded by the modulation doped structures, such as the VHEMT are also important features for the now common high speed HEMTs. The cross-sectional energy band diagram of an n-channel AlGaAs/GaAs HEMT utilizing a two dimensional electron gas (2DEG) is shown in figure 4. The potential notch at the AlGaAs/GaAs interface confines the electrons to a region about 50-100A° thick which leads to a formation of a pseudo-triangular quantum well. Quantized energy levels are formed in this triangular well, with the first subband fully occupied and the second subband generally partially filled. The Fermi level is placed between the first and the second subband reflecting the degeneracy of the 2DEG system, leading to a drift mobility of these electrons that appears to be equal to the phonon limited mobility. This leads to extremely small parasitic resistances. Therefore in HEMTs, large currents can be switched at very high speeds resulting in shorter capacitor charging times and lower power consumption. Unfortunately the HEMTs based on AlGaAs/GaAs heterostructures have several limitations:

(1) When a HEMT with drain to source voltage bias less than 0.5V, is cooled to 77K without exposure to light, the current in the channel drops to about zero. This is known as the drain current collapse, and arises from the capture of electrons by the defects induced by donors (DX Centers) in AlGaAs with large Al mole fractions. The capture occurs primarily when the electrons are injected into the AlGaAs near the drain and reduces the net positive space charge which in turn depletes the 2DEG and restricts current flow in the channel.

(2) The sheet carrier concentration is limited to below $10^{12}cm^{-2}$ per interface which determines the upper limit for

the current. Larger Al mole fraction are required to increase the sheet carrier concentration. However, this results in increased defect concentration and donor binding energy which increases the current collapse.

(3) The electron velocity in GaAs is lower than in other semiconductors. For example InGaAs alloys exhibit higher electron velocities and the enhancement of these velocities at lower temperatures far exceeds that of GaAs.

In an AlGaAs/GaAs HEMT the effect of DX centers can be minimized by reducing the mole fraction of Al below 15%. Unfortunately this results in a small bandgap discontinuity (120 meV) which reduces significantly the sheet carrier concentration. Thus in order to maintain high 2DEG concentration and minimize the effect of drain current collapse, it is necessary to maintain a large bandgap discontinuity. This could be accomplished by using a semiconductor with a smaller bandgap in the region (approximately 100-150A° wide layer) where the 2DEG is confined. Fortunately, InGaAs alloys have smaller bandgap and exhibit superior velocity field characteristics, so that higher performance is expected. However, because the lattice constant of InGaAs is larger than GaAs, the thickness and composition of the InGaAs layer should be carefully designed to accommodate the strain caused by the mismatch.

The pseudomorphic HEMT shown in figure 5 was developed as a result of addressing the above problems through a joint effort between the University of Illinois and General Electric [7]. This PHEMT had extrinsic transconductance that was as high as 495 mS/mm at 300K (recent results of 1000mS/mm have been reported), with power levels of 0.43 W/mm at 62 GHz and power added efficiency of 20%. From the power gain measurements at 62 and 94 GHZ it was concluded that the device could provide power gain up to 230 GHz. Additionally, maximum gains achieved at 62 GHz and 94 GHz were 11.7 dB and 7 dB, respectively. Comparatively, the GaAs/AlGaAs HEMT which has undergone many years of optimization show about 7dB gain at 60 GHZ. For the PHEMT, optimization and further reduction in gate length should lead to higher power gains and higher frequency of operation. Some of the basic question that should be addressed to develop the PHEMT with the ultimum performance are:

(1) What is the effect of gate length on device characteristics?

(2) What is the effect of increasing the In mole fraction in the InGaAs layer? Since InGaAs has the smaller band gap, will this translate to better performance?

(3) What is the optimum InGaAs layer thickness and what is the corresponding doping level in AlGaAs layer?

(4) How will the device characteristics change if other materials are used, e.g. InP instead of GaAs.

Accurate numerical simulation studies can answer the above questions for both the VHEMT and the PHEMT and provide information on device characteristics prior to fabrication. Such a study can also provide information on the transient behavior of these structures that can be related to the

instrumentation used to characterize these devices. This report describes the first numerical study undertaken to address such issues as they relate to the VHEMT and the PHEMT. In addition this study also addresses, through numerical simulation, the key issue of interpreting measurements that purport to measure the speed of electronic devices. In this Phase I study an empricial definition of speed is introduced below, and an assessment of the measurements of the Mourou group at the University of Rochester, as they relate to this definition is discussed. Accordingly, these issues identify the key technical objectives of the Phase I SBIR study.

2. PHASE I TECHNICAL OBJECTIVES

The Phase I technical goals were to implement SRAs MINT (multidimensional implicit nonlinear time-dependent) algorithm:

(1) to simulate the dc electrical behavior of the vertical and pseudomorphic HEMTs,

(2) to ellucidate the device physics and transport characteristics of these structures; and

(2) to pulse the gate of the pseudomorphic HEMT to simulate the broad features of the University of Rochester (UR) transient measurements, and thereby assess the extent to which the UR group measures the speed of electronic devices.

3. ANALYSIS

3.1 Governing Equations.

To achieve the stated goals of this study the drift and diffusion equations, as given below, were solved. Here, the governing continuity equations take the form:

$$\frac{\partial N}{\partial t} = \frac{1}{e} \nabla \bullet J_n + G - R \tag{1}$$

$$\frac{\partial P}{\partial t} = - \frac{1}{e} \nabla \bullet J_p + G - R \tag{2}$$

where the current densities are given by:

$$J_n = e\left(N\mu_n \nabla(\psi+\phi_n) - D_n \nabla N\right) \tag{3}$$

$$J_p = -e\left(P\mu_p \nabla(\psi+\phi_p) + D_p \nabla P\right) \tag{4}$$

The quantities ϕ_n and ϕ_p are introduced to account for variations in the conduction and valence band energy levels, and are related to the electron affinity, the density of states and the energy band gap as [10]:

$$\phi_n = \frac{1}{e} (\chi + kT \ln N_c) \tag{5}$$

$$\phi_p = \frac{1}{e} (\chi + E_g - kT \ln N_v) \tag{6}$$

The gradients of ϕ_n and ϕ_p give rise to local "effective fields" at material interfaces which may augment or retard drift transport across the interface. G and R in Eqs. (1) and (2) are generation and recombination terms. The recombination term is given as:

$$R = \frac{NP - N_i^2}{\tau_p(N+N_i) + \tau_n(P+N_i)} + r(N+P)(NP-N_i^2) \tag{7}$$

Here τ_n and τ_p are recombination lifetimes whereas r is a recombination rate constant. The first and second terms in Eq. (7) represent Shockley-Read-Hall and Auger recombination, respectively. For GaAs, the carrier lifetimes are on the order of 1 nsec.

Since space charge effects must be considered in the present analysis, a self-consistent electric field must be determined from Poisson's equation

$$\nabla \cdot \epsilon \nabla \psi = -\rho = e(N-P-C) \tag{8}$$

where C is the net doping distribution of donor and acceptor ions. Here we note that, due to the heterojunction formulation, the permittivity could be spatially dependent.

3.2 Mobility and Diffusivity Models.

The mobility model used in the present simulations allows for negative differential mobility of GaAs electrons. The electron velocity is given by:

$$V_n = [\mu_o F + a(F/F_v)^2 + b(F/F_v)^3 + c(F/F_v)^4] \frac{1}{1 + (F/F_v)^4} \tag{9}$$

where μ_o is the low field mobility, F_v, the electric field at peak velocity. The field F is the magnitude of the negative gradient of $\psi + \phi_m$.

The diffusivity is then determined using the Einstein relation:

$$D = \frac{kT}{e} \mu \tag{10}$$

where k is Boltzmann's constant, and T is the temperature (taken here as constant, 300°K). The constants used in the velocity expression for GaAs/$In_{0.15}Ga_{0.85}As$ and $Al_{0.15}Ga_{0.85}As$ are given in Table 1.

3.3 Boundary Conditions and Doping Specification.

The specification of the doping distribution and the boundary conditions determine the type of device under consideration and the bias point. For the two dimensional simulations considered here, the device structure is taken as two-dimensional in the X-Z plane. The doping distribution for the device is thus given as:

$$C(x,z) = N_D - N_A \tag{11}$$

Boundary conditions are required for ohmic contacts and free surfaces. The carrier densities at ohmic contacts are determined through the assumption of zero space charge:

$$N - P = C \tag{12}$$

together with the assumption of thermal equilibrium:

$$NP = N_i^2 \tag{13}$$

The concentrations of electrons and holes at ohmic contacts, as well as the initial distribution of carriers throughout the device, are determined by simultaneous solution of Eqs. (12 and 13).

The potential at ohmic contacts is specified relative to the vacuum level, as it must be if a consistent treatment of heterojunctions is to be retained.

At N-type contacts:

$$\Psi = V_{APP} + \frac{kT}{e} \ln \frac{N}{N_C} - \frac{\chi}{e} \tag{14}$$

and at P-type contacts:

$$\Psi = V_{APP} - \frac{kT}{e} \ln \frac{P}{N_V} - \frac{E_g}{e} - \frac{\chi}{e} \tag{15}$$

It should be noted that in the absence of any variation in the electron affinity, and under the assumption that the Fermi level is centered between the conduction and valence bands (i.e. $N_c = N_v$), Eq. (14), for example, reduces to the commonly used relationship for homojunctions,

$$\Psi = V_{APP} + \frac{kT}{e} \ln \frac{N}{N_i} \tag{16}$$

where the contributions to the built-in potential from the band gap and electron affinity are ignored since they are equal at all contacts.

At free surfaces, the normal component of electric field and current density are set to zero.

4. THE NUMERICAL METHOD

4.1 Philosophy of the Solution Procedure:

A detailed discussion of the solution technique, including the development of consistent difference approximations to the governing equations, is given in [8]. Thus, the discussion here will be limited to the philosophy behind the technique and implementation on a vector machine.

In an effort to develop a highly efficient solution technique to the system of Eqs. (1, 2 and 8) it is first recognized that this system is a coupled, non-linear system. If solved as a coupled system, it will require utilization of methods designed for coupled elliptic equations to obtain a solution at each time step. These methods typically introduce some outer iteration to treat nonlinearity and the methods used to solve the difference approximations to the linearized system are often computationally intensive in two dimensions, and totally impractical to implement in three. By contrast, the method used here eliminates nonlinear iteration, uses a noniterative yet highly efficient procedure to solve the difference approximations to the continuity equations, and uses an extremely efficient iterative technique to solve the equation governing the potential. As shall be discussed, these solution techniques are also ideally suited for implementation on vector machines and/or parallel processors making them even more attractive.

The first step in this procedure is to decouple Poisson's equation from the continuity equation in a manner which does not adversely effect stability of the overall solution algorithm. This is accomplished by reformulating the continuity equations by expanding the drift term, and substituting the space charge for the Laplacian of the potential. After manipulation, the result is

$$\frac{\partial N}{\partial t} = -\nabla \cdot N\mu_n \nabla F_n - \nabla \mu_n N \cdot \nabla \psi - \mu_n \frac{Ne}{\epsilon} \quad \text{(N-P-C)}$$

$$+ \mu_n \frac{N}{\epsilon} \nabla \epsilon \cdot \nabla \psi + \nabla \cdot D_n \nabla N + G - R \tag{17}$$

$$\frac{\partial P}{\partial t} = \nabla \cdot P\mu_p \nabla F_p + \nabla \mu_p P \cdot \nabla \psi + \mu_p \frac{Pe}{\epsilon} \text{ (N-P-C)}$$

$$- \mu_p \frac{P}{\epsilon} \nabla \epsilon \cdot \nabla \psi + \nabla \cdot D_p \nabla P + G - R \tag{18}$$

To ensure conservation of total current, Poisson's equation is recast as a statement of total current,

$$\frac{\partial \nabla \cdot \epsilon \nabla \psi}{\partial t} = - e\nabla \cdot N\mu_n \nabla(\psi + F_n) - e\nabla \cdot P\mu_p \nabla(\psi + F_p)$$

$$+ e\nabla \cdot (D_n \nabla N - D_p \nabla P) \tag{19}$$

From Eqs. (17-19) it is easily shown that at steady state, Poisson's equation is satisfied exactly. A small error is introduced in transients, as discussed in [8].

Eqs. (17-19) form the basis of the solution algorithm. To advance the solution from t^n to $t^{n+1} = t^n + \Delta t$, the mobilities and diffusivities are evaluated using the electric field and carrier densities at t^n. Additionally, the gradients of potential appearing in the second and fourth terms on the R.H.S. of Eqs. (17 and 18) are evaluated at the t^n level. This effectively decouples the continuity equations from the total current constraint and allows the carrier concentrations to be advanced first. This decoupling does not introduce a stability constraint [8].

The advance in time of the carrier concentrations is performed by solving the continuity equations (Eqs. (17 and 18)) as a block 2x2 coupled system through application of a linearized block implicit (LBI) method [9]. The continuity equations are of the form

$$\frac{\partial \phi}{\partial t} = D(\phi) + S(\phi) \tag{20}$$

where $\phi = (N,P)^T$, $D(\phi)$ represent those terms in Eqs. (17 and 18) which contain spatial derivatives of ϕ, and $S(\phi)$ represent source terms such as the recombination, generation and space charge terms. Eq. (20) is then time differenced using a backwards differencing scheme,

$$\frac{\Delta \phi^{n+1}}{\Delta t} = D(\phi)^{n+1} + S(\phi)^{n+1} + O(\Delta t) \tag{21}$$

where $\Delta\phi^{n+1} = \phi^{n+1} - \phi^n$, and the superscripts refer to the time level. $D(\phi)^{n+1}$ and $S(\phi)^{n+1}$ are then formally linearized in time using a Taylor series expansion about the solution at time t^n as:

$$G(\phi)^{n+1} = G(\phi)^n + \Delta t \left.\frac{\partial G(\phi)}{\partial \phi}\right|^n \left.\frac{\partial \phi}{\partial t}\right|^n + O(\Delta t^2) \tag{22}$$

Substituting a forward difference approximation for the time derivative in Eq. (21):

$$G(\phi)^{n+1} = G(\phi)^n + \left.\frac{\partial G(\phi)}{\partial \phi}\right|^n \Delta\phi^{n+1} + O(\Delta t^2) \tag{23}$$

Eq. (26) may then be expressed as:

$$(A + \Delta t L)\Delta\phi^{n+1} = \Delta t\left[D(\phi)^n + S(\phi)^n\right] + O(\Delta t) \tag{24}$$

where:

$$A = I - \Delta t \left.\frac{\partial S(\phi)}{\partial \phi}\right|^n \tag{25}$$

and:

$$L = - \left.\frac{\partial D(\phi)}{\partial \phi}\right|^n \tag{26}$$

When the L operator is approximated by three-point difference approximations Eq. (24) represents a block 2x2 matrix equation which may be written at each grid point in the solution domain. In one dimension, the result is a block 2x2 tridiagonal coefficient matrix which may be solved efficiently using direct block tridiagonal elimination. For two- or three-dimensional approximations, while the block size remains 2x2, since it is determined by the number of coupled equations, the bandwidth of the resulting coefficient matrix increases significantly. In two dimensions, on a square mesh of NxN points, the rank of the coefficient matrix is of order N^2 and the bandwidth is of order N. In three dimensions, with an NxNxN mesh, the rank of the coefficient matrix is of order N^3 and the bandwidth of order N^2. Obviously, use of direct inversion techniques for such matrices, for even relatively small meshes, would result in a computationally intensive and inefficient solution procedure. For this reason, iterative matrix solvers are often used. However, for large meshes even these iterative solvers may become prohibitive and should be avoided, if possible. This can be accomplished, due to the parabolic nature of continuity equations, by applying a consistently split ADI procedure [10] to solve Eq. (24). To split or factor Eq. (24), the L operator is separated into its directional components, $L = L_x + L_y + L_z$, and Eq. (24) is rewritten as a sequence of one-dimensional systems along each mesh line in the x, y and z directions respectively:

$$(A + \Delta t L_x)\Delta\phi^* = \Delta t\left[D(\phi)^n + S(\phi)^n\right] \tag{26}$$

$$(A + \Delta t L_y)\Delta\phi^{**} = A\Delta\phi^{*} \tag{26}$$

$$(A + \Delta t L_z)\Delta\phi^{***} = A\Delta\phi^{**} \tag{26}$$

Elimination of the intermediate steps in Eq. (32) yields:

$$(A + \Delta t L_x)A^{-1}(A + \Delta t L_y)A^{-1}(A + \Delta t L_z)\Delta\phi^{***} = \Delta t\left[D(\phi)^n + S(\phi)^n\right] \tag{27}$$

Comparison of Eqs. (24 and 27) shows that Eq. (27) approximates Eq. (24) to $0(\Delta t^2)$, thus:

$$\Delta\phi^{n+1} = \Delta\phi^{***} + 0(\Delta t^2) \tag{28}$$

While this factorization error may place additional restrictions on the time step when considering accuracy, the overall reduction in computational effort will typically more than offset this limitation. Each of Eqs. (26) is tridiagonal, thus direct elimination can be implemented in a highly efficient manner. On an NxNxN mesh, the factorization reduces the need to solve a rank N^3 matrix to a task requiring the solution of $3N^2$ tridiagonal matrices of rank N. Since only tridiagonal matrices need to be solved, regardless of the mesh structure, the number of operations per mesh point remains constant and the computational effort required to solve the continuity equations varies linearly with total mesh points when implemented on a scalar machine.

Having advanced the carrier concentrations, the total current constraint, Eq. (19) must be solved for the potential. Since the carrier densities at t^{n+1} are now known, Eq. (19) can be differenced fully implicitly while only ψ remains unknown. It must be noted that while a time derivative appears in Eq. (19), this equation remains elliptic and must be solved iteratively. To accomplish this Eq. (19) is recast as:

$$\rho\Delta\psi = \frac{\partial\nabla\bullet\epsilon\nabla\psi}{\partial t} + e\nabla\bullet N\mu_n\nabla(\psi + F_n) + e\nabla\bullet P\mu_p\nabla(\psi + F_p) - e\nabla\bullet(D_n\nabla N - D_p\nabla P) \tag{29}$$

and Eq. (29) expressed as:

$$(A + \frac{1}{\rho}L)\Delta\psi^{i+1} = \frac{1}{\rho}\left[D(\psi)^i + S(\psi)^i\right] \tag{30}$$

where:

$$A = I - \frac{1}{\rho}\left.\frac{\partial S(\psi)}{\partial\psi}\right|^i \tag{31}$$

and:

$$L = - \left. \frac{\partial D(\psi)}{\partial \psi} \right|^{i} \tag{32}$$

Here, $D(\psi)$ includes the first three terms on the R.H.S. of Eq. (29) and $S(\psi)$ the last term. The superscript "i" refers to an iteration index and ρ is an acceleration parameter which varies both spatially and from iteration to iteration. Eq. (30) may be ADI split, as were the continuity equations, following Eqs. (26). However, in contrast to the continuity equations, the total current constraint must be iterated to convergence at each physical time step. With the proper choice of acceleration parameters this can be accomplished rapidly and efficiently. It should also be noted that since the D operator is linear in ψ, L = -D and the D operator need only be computed at the start of the iteration and stored. Similarly, the S operator is not a function of ψ in this case, thus $\partial S/\partial \psi = 0$. The S operator also need be computed only once and stored. At convergence, $\Delta\psi^{i+1} = \Delta\psi^{***}$ will go to zero and, as may be observed from Eq. (27), the factorization error will also go to zero and the difference approximations to Eq.(19) is solved exactly. This completes the advance of the solution from t^n to t^{n+1}. The process is then repeated for the next time step.

5. RESULTS

The steady state characteristics of the VHEMT and the PHEMT were calculated using two dimensional numerical solutions of the drift and diffusion equations as outlined in the previous section. Additionally, the transient response of the PHEMT to time dependent voltage pulses with different shapes and duration superimposed on the gate were computed using a transient accurate numerical algorithms. The latter situation resembles the electro-optic sampling approach used by Mourou's group to measure the speed of response of HEMT and PBT. The structures of both the VHEMT and PHEMT used in the investigation and the results of the simulation are discussed next.

5.1 Vertical HEMT (VHEMT)

5.1.1 Device and Grid Structure:

The structure of the VHEMT studied in this Phase I is depicted in figure 3-b. The separation between the drain and the source is 1μm, and the full length of the drain contact is 1μm and that of the source is 0.5μm. The ohmic source contact is assumed to be in direct contact with the AlGaAs layer to simplify the computation. The Schottky gate contact is 100nm long and is located 50nm away from the corner on the vertical AlGaAs surface. The AlGaAs layer is doped $1x10^{18}$ cm^{-3} and is grown on top and to the side of an undoped GaAs layer whose thickness varies from 50nm below the source to 115 nm to the side of the gate. A GaAs layer doped $3x10^{16}$ cm^{-3} is grown on top of the highly doped ($6x10^{17}$ cm^{-3}) GaAs layer to which the drain contact is attached. The lightly doped GaAs layer form a centrally located channel that provides a current path at low and reverse gate biases.

The grid structure shown in figure 7 was used in the numerical simulation of the VHEMT. The grid is variable in spacing and includes a more densely packed mesh at all junctions and the depletion region around the gate. The total number of grid points included 88 points in a direction normal to the drain and 52 in a parallel direction. The smallest grid spacing was lnm near the

heterojunction. For a given set of bias levels Vgs and Vds, the computer code was used to obtain steady state results for current and distribution of space charge and potential. The material parameters of $Al_{0.2}Ga_{0.8}As$ and GaAs are summarized in table 2.

5.1.2 Electrical Characteristics:

The I-V characteristics of a 100μm wide VHEMT is shown in figure 8a. Significant drain current begins to flow at drain biases above 0.2V. The interesting feature in the I-V characteristics is the large values of drain current even when the gate is reverse biased by 0.5V. The highest value of current, for the range of bias investigated, is 18mA at V_{ds} = 2.0V and V_{gs} = 0.5V. To determine the negative bias voltage on the gate required to pinch off the channel completely (i.e. zero drain current), several calculations were performed at drain bias of 2.0V for gate biases between -7.0V and 0.5V. The drain current is plotted in figure 9a as a function of the gate bias voltage. It is clear that the drain current turns off very slowly and requires a very high reverse gate bias of 7.0V. To highlight this result the transconductance as a function of the gate bias is plotted in figure 9b for a drain bias of 2.0V. The transconductance varies from 10 mS/mm to 94 mS/mm. These values of transconductance are very small compared to those obtained for pseudomorphic HEMT which has experimentally measured values as high as 1000 mS/mm.

The small values of the transconductance are attributed to the presence of lightly doped central channel which provides a current path that is difficult to control by the gate. This difficulty arises because the electrons in the undoped GaAs layer adjacent to the AlGaAs/GaAs abrupt junction are subjected to an electric field that attracts them towards the interface. Additionally the change in the doping from π-GaAs to $3x10^{16}$ cm^{-3} n-type results in a built-in potential that must be overcome before depletion can occur.

In addition to the current-voltage and transconductance relationships, current streamlines, potential and charge distributions were obtained. The current streamlines are plotted in figures 10 and 11. We note that between each streamline flows equal amounts of current density. Figures 10 and 11 show that as the bias voltage on the gate is reduced from 0.5V to -5.0V, the percentage of the current passing through the central channel increases from 20% to 90% of the total current corresponding to that gate bias, although in the latter case the current is small. The figures also show that the presence of the horizontal AlGaAs/GaAs below the gate increases the current flow lines (i.e., the electrical path length is increased) because the electrons are subjected to an electric field that constrains them to move parallel to the interface especially near the corner. Further evidence for this is contained in the potential plots.

Figure 12 shows a plot of equipotentials indicating that electrons near the corner below the gate are subjected to an electric field that forces the electrons to move parallel to the horizontal interface instead of moving towards the drain. However, in the central channel region the electron motion is one dimensional as can be seen from the fact that the equipotential lines are perpendicular to the gate plane. Consequently, the dominant component of the electric field force is parallel to the gate plane which leads to the straight and short current flow lines in the central channel region as can be seen in figures 10 and 11. It is also obvious from these figures that using an undoped central channel region will reduce the current flow in that region and is likely to bend the current streamlines near the source, unless the heterointerface is eliminated. This factor has not been investigated in this study and should be addressed in an anticipated phase II study.

In order to further understand the characteristics of the VHEMT such as the I-V and the large reverse bias voltage required to pinch off the channel, the electron distribution in selected regions of the device was examined. Figures 13 and 14 show the variation of the electron concentration along a line perpendicular to the gate from the gate contact to the line of symmetry (see figure 3b) for gate biases of 0.5V, 0.0V, -0.5V, and -5.0V. Figure 13a shows that even at forward bias of 0.5V on the gate the electron population within the first 20 nm is less than $1x10^{16}$ cm^{-3} which is two order of magnitudes below electron concentration near the source. This thickness amounts to more than 50% of the AlGaAs layer thickness. Therefore in order to obtain the higher current densities provided by the high doping of the AlGaAs layer, higher forward bias on the gate is required to increase the fraction of this layer available for current flow. The figure also shows that the maximum electron concentration reaches about $6x10^{17}$ cm^{-3} at the heterojunction within the GaAs layer. The electron density then drops gradually and reaches a minimum of $3x10^{16}$ cm^{-3} at a distance of 100 nm from the interface in the undoped GaAs layer. The electron concentration in the central channel reaches $5x10^{16}$ cm^{-3} which is above the background doping level of $3x10^{16}$ cm^{-3}.

As the bias on the bias on the gate is reduced from 0.5V to 0.0V the electron concentration in the AlGaAs/GaAs interface drops to about $1x10^{17}$ cm^{-3} as shown in figure 13b down from $6x10^{17}$ cm^{-3} at 0.5V on the gate. The electron concentration beyond 100 nm from the gate remains essentially the same as before. When the gate bias is decreased to -0.5V, the AlGaAs layer is completely depleted and the electron concentration in heterointerface drops to about $1x10^{14}$ cm^{-3} as can be seen in figure 14a. The electron concentration then increases rapidly to $1x10^{16}$ cm^{-3} at 12nm from the interface and gradually increases to $5x10^{16}$ cm^{-3} at the central channel region. Figure 14b shows that further decrease in the gate bias to -5.0V drastically depletes the device such that the electron concentration is below 1.10^{14} cm^{-3} within 150 nm distance from the gate. The electron concentration then increases gradually to reach $2x10^{16}$ cm^{-3} at a distance of 225 nm from the gate. Thus the effective channel width through which current can flow at this bias level is about 25 nm. This explains the significant crowding of the current streamlines in figure 11b, which

corresponds to -5.0V bias on the gate. Additionally it clearly demonstrates that doping of the central layer is responsible for increasing the reverse bias on the gate required to completely pinch off the channel.

Contour plots of electron concentration are shown in figure 15. These plots display an accumulation layer in the central channel below the gate corresponding to this increased electron concentration. However, the electron concentration decreases to the background doping level as one moves towards the source or drain. We note that these details may be model dependent, in that the transport model used in this calculation, is based on the drift and diffusion model and totally ignores the nonequilibrium nature of the electron transport in this region. Earlier simulations of the PBT by Bozler [11] and Osman [5] using the drift and diffusion model report the same effect. However, later calculations by Hwang [12] using the Monte Carlo method and Kreskovsky et al [13], using the moments of BTE show no such accumulation in the region of the device. Therefore more realistic device parameters for the VHEMT can be obtained only when the nonequilibrium nature of the electron transport is taken into account in addition to quantization of the electron gas in the undoped GaAs layer adjacent to the AlGaAs/GaAs interface.

The variation, with gate bias, of the electron concentration in the region between the drain and the highly doped AlGaAs layer, along the two lines denoted by 1 and 2 in the VHEMT device structure in figure 3b, is plotted in figures 16 and 17. The interesting feature in these figures is the fact that the carrier concentration in the undoped GaAs layer along line 2 is always larger than $1x10^{16}$ cm^{-3}, even for a reverse bias of -5.0V on the gate. Additionally, there is always charge accumulation in the undoped GaAs layer adjacent to the AlGaAs/GaAs interface. This shows that the presence of the heterojunction confines the electrons near the interface even in the presence of a 2V bias on the drain. Operating the device at higher drain bias voltages will result in a stronger electric field that attracts the electrons to the drain and might lead to less electrons being confined at the interface. However, the validity of this prediction can only be tested by simulating the device at higher drain bias conditions. This could be done in an anticipated Phase II program. The electron concentration in the AlGaAs layer is equal to background doping level except close to the heterointerface where the concentration drops to $2x10^{17}$ cm^{-3} for 0.2V and 0V gate biases as shown in figures 16a and 16b. Figure 17b shows that when the gate bias is decreased to -5.0V, the electron concentration near the surface of the AlGaAs layer along line 1 drops to $2x10^{15}$ cm^{-3} and then increases to $1x10^{17}$ cm^{-3} at a distance of 25 nm from the surface. The electron concentration in the undoped GaAs reaches $1x10^{17}$ cm^{-3} at the interface and drops rapidly to below $1x10^{15}$ cm^{-3} and then increases gradually to $1x10^{17}$ cm^{-3} at the n/n^{+} junction near the drain. The minimum of electron concentration in the undoped GaAs layer along line 1 decreases from above $1x10^{16}$ cm^{-3} to below $1x10^{15}$ cm^{-3} as the gate bias is decreased from 0.5V to -5.0V. However, the concentration along line 2 remains always above $1x10^{16}$ cm^{-3} and is not sensitive to the gate bias. The fact that the electron concentration is higher along line 2 compared to line one implies that the device exhibits lower resistance to the electron current along line 2. Consequently, the current streamlines bend after they pass the gate region to reach those low resistance regions. The current streamlines then become

straight lines normal to the drain plane because the motion of electrons is almost one dimensional under the influence of an effective electric field that attracts the electrons to the drain.

A three dimensional color distribution of the electron concentration inside the VHEMT for a gate bias of 0.5V is shown in figure 18. The plot shows that the electron concentration in the highly doped GaAs layer near the drain and in the AlGaAs layer in near the source and away form the gate are essentially equal to the background doping level. It also shows the depletion in region near the gate. Additionally, it shows how the undoped GaAs layer physically separates the drain from the highly doped AlGaAs layer. Ideally a high doping in this region, or decreasing the thickness of the undoped layer can result in higher electron density. This can lead to higher drain current levels due to the decrease in the resistance of the semiconductor layer between the drain and the AlGaAs layer. This effect should be more significant at higher forward gate bias voltages, when a significant portion of current flows through the highly doped AlGaAs layer. A thorough numerical simulation that takes into account the two dimensional nature of the electrons at heterointerface, degeneracy in the AlGaAs layer, and the nonequilibrium transport of the electrons in the high field regions is required to achieve better understanding of the VHEMT characteristics. This can give more realistic estimates of the relative contributions of the 2DEG and the electrons in the AlGaAs to the total current and provide the means to optimize the electrical characteristics of the VHEMT.

In summarizing the results of the VHEMT study we must point out that the results are specific to design considered. The concept of the VHEMT in which both FET and HEMT like modes of operation are possible, remains attractive provided some of the issues addressed below are resolved:

1. The lightly doped central channel layer provides a current path that is difficult to pinch off and leads to lower transconductance. The bias required for pinch off is very high compared to a PBT with the same dimensions due to the following factors:

   (a) The high doping of the AlGaAs layer screens the effect of the Schottky barrier gate by reducing the depletion layer thickness. Consequently a high reverse bias is required to extend the gate control to the GaAs layer.

   (b) The band bending in GaAs layer adjacent to the AlGaAs/GaAs interface pulls the electrons towards the interface to form the 2D electron gas, where as the reverse bias on the gate tends to deplete the electrons. As a result a higher reverse bias is required to deplete the channel layers.

   (c) The abrupt change in doping profile from undoped GaAs layer to N = 3 x $10^{16}cm^{-3}$ doping in the central channel region results in a built-in potential that works against reverse bias voltages on the gate. Thus an additional bias on the gate is required to overcome the built potential before attempting to deplete the central channel layer. Using the expression for the built-in potential, $V_{bi} = (kT/q)\ln[N_A + N_D/n_i^2$ [14]. With $N_A = 10^{14}cm^{-3}$, $N_D = 3 \times 10^{16}cm^{-3}$, $n_i = 1.79 \times 10^{6}cm^{-3}$, and T = 300K,

the value of V_{bi} is 1.07ev. This means that the presence of the junction requires an additional 1 volt reverse bias on the gate.

2. The high mobility and high concentration of the two dimensional electron gas in the channel are not fully utilized in the present form of the VHEMT. These two properties are the key factors in the superior performance of the HEMT relative to other devices. In all current HEMT structures the electrons traverse below the gate and arrive at the highly doped drain contact where they are collected. On the other hand, the electrons in the VHEMT cross the region below the gate as in any present HEMT and then have to traverse a low doped GaAs region which presents a high resistance to current flow. Furthermore, they have to overcome the electric field that confines the electrons close to the AlGaAs/GaAs interface. The net effect is a longer path for the current flow compared to both the PBT and HEMT.

5.2 Pseudomorphic HEMT (PHEMT):

5.2.1 Device and Grid Structure:

The device structure of the PHEMT studied in this Phase I SBIR is shown in figure 5. The structure consists of a 1-μm thick unintentionally GaAs buffer layer, followed by a 15 nm thick $In_{0.15}Ga_{0.85}As$ layer, 3 nm of undoped $Al_{0.15}Ga_{0.85}As$ as a spacer layer, and 35 nm of N^+ $Al_{0.15}Ga_{0.85}As$ doped $1x10^{18}$ cm^{-3}. The source and drain ohmic contacts are 0.5 μm long and are taken to be in direct contact with the highly doped AlGaAs layer to simplify the computation. The Schottky gate is 0.25 μm long and is centrally placed.

In order to obtain the electrical characteristics of the PHEMT and understand the operation of the device using numerical simulation, the grid structure shown in figure 19 was employed. The grid is variable in spacing and includes a more densely packed mesh at all junctions and in the gate depletion region.

The total number of grid points included 76 points from the contacts plane to bottom end of the undoped epitaxial GaAs layer and 73 points from the source contact to the drain contact. The smallest grid spacing used was lnm in the AlGaAs layer and the heterojunction region. The computer code was then used to obtain the steady state values for the current, space charge, and potential distribution at given set of bias levels Vgs and Vds. Additionally, the transient response for a time varying voltage pulse on the gate was determined using a transient accurate algorithms. The material parameters for $Al_{0.15}Ga_{0.85}As$ and $In_{0.15}Ga_{0.85}As$ used in the computation are summarized in table 2.

5.2.2 Electrical Characteristics:

The I-V characteristics of a 50 μm wide PHEMT are shown in figure 20a. The device shows an enhancement in the transconductance with more forward bias on the gate. The transconductance in the forward direction reaches a maximum of

372 mS/mm at a drain bias of 3.0V as can be seen in figure 20b. On the other hand, the transconductance for the reverse bias is smaller and reaches a maximum of 190 mS/mm at a drain bias of 3.0V. The experimental value for the transconductance is about 475 mS/mm for PHEMT with the same dimensions and a higher doping level of $3x10^{18}$ cm^{-3}. The higher experimental transconductance compared to the computed value is due to the differences in the doping levels of the AlGaAs layer and the neglect of the nonequilibrium nature of the electron transport, particularly in the InGaAs channel layer, and the high field regions. The PHEMT values of the transconductance are considerably higher than the corresponding values for the VHEMT.

In order to understand the origins of the high performance of the PHEMT, the electron distribution along selected lines in the device were plotted to display the spatial and bias dependence of the charge distribution. The variation of the electron concentration along lines normal to the source, gate, and drain are plotted in figure 21 for a gate bias of 0.2V and drain bias of 1.0V. Figure 21a shows that normal to the source center, the electron concentration within the first 30 nm of the AlGaAs layer remains equal to the background doping level. However, throughout the remaining 5-8 nm the electron concentration drops gradually and reaches a minimum of $4x10^{17}$ cm^{-3} near the AlGaAs/InGaAs interface. The density then increases rapidly to $1.5x10^{18}$ cm^{-3} within the InGaAs channel layer adjacent to the heterojunction and then drops to about $3x10^{16}$ cm^{-3} over a very short distance (3-4nm). Within the remaining thickness of the channel (10nm) the density drops gradually to $1x10^{16}$ cm^{-3} at the InGaAs/GaAs interface. Another very drastic drop in the electron density occurs as one crosses the InGaAs/GaAs interface. The density changes from about $1x10^{16}$ cm^{-3} in the InGaAs channel to well below $1x10^{14}$ cm^{-3} in the GaAs substrate. The confinement of the electrons to the InGaAs layer improves the performance of the PHEMT because it leads to shorter electron path from the source to the drain. Additionally, under zero gate bias conditions, the electric field is very small in this region and most of the electrons in the InGaAs channel are confined near the AlGaAs/InGaAs interface.

The charge distribution along a line normal to the gate center is plotted in figure 21b. Within the first 20 nm distance from the Schottky gate contact,

the electron density remains below $1x10^{16}$ cm^{-3} and is increasingly depleted as one move closer to the gate. This arises because the Schottky barrier height is 0.9V, so that even when there is a forward bias on the gate of 0.2V the net electric potential felt by the electrons is -0.7V and repels the electrons away from the regions close to the gate. As one moves away from the gate to the heterojunction, the electron density increases gradually to reach a maximum of $4x10^{17}$ cm^{-3} at a distance of 4-5 nm from the interface and then decreases to about $3x10^{17}$ cm^{-3} at the interface. Within the InGaAs layer, the density rises rapidly to $1x10^{18}$ cm^{-3} and drops back to $3x10^{17}$ cm^{-3} within 2-3 nm from the AlGaAs/InGaAs interface. Subsequently, the density drops gradually to about $6x10^{16}$ cm^{-3} at the InGaAs/GaAs interface and undergoes a sharp drop to about $1x10^{15}$ cm^{-3} in the GaAs substrate. Comparing the charge distribution along this line to that in the source region, we find that the electron concentration within the AlGaAs layer and at the AlGaAs/InGaAs interface is

higher under the source. However, within most of the InGaAs channel and at the InGaAs/GaAs interface the electron concentration is higher under the gate region than under the source region. Also the electron density in the GaAs substrate under the gate are two to three orders of magnitudes higher compared to that under the source. This different behavior arises because of a combination of several effects: (1) The electrons under the gate are subjected to a strong repulsive force from the Schottky gate contact, and consequently are depleted near the gate and are pushed away from the AlGaAs/InGaAs interface to the center of the channel and the GaAs substrate. (2) The presence of the potential barrier at the InGaAs/GaAs interface significantly reduces the fraction of electrons that escape to the GaAs substrate. (3) The constraints of current continuity combined with the above two conditions lead to the high current density and the superior switching properties of the PHEMT compared to the HEMTs based on the AlGaAs/GaAs alone.

The variation of the electrons density within the AlGaAs layer along a line normal to the drain (see figure 21c) is similar to that in the source region. However, the electron density at the AlGaAs/InGaAs interface within the InGaAs channel is smaller than the corresponding value under the source. This is attributed to the attractive force exerted by positive drain bias on the electrons and the diffusion of electrons to the GaAs substrate as they reach the drain end of the channel after being subjected to the repulsive electric force under the gate. Within the channel the density drops from 1x1018 cm^{-3} to about $2x10^{16}$ cm^{-3} over a short distance of 6 nm and stays almost constant up to the InGaAs/GaAs interface. A sharp drop to $7x10^{15}$ cm^{-3} in GaAs substrate occurs as one crosses the interface. The electron concentration then decreases gradually to $2x10^{15}$ cm^{-3} over a distance of 25 nm. Thus we see that the significant feature of the electron distribution near the drain is the larger density in the InGaAs channel and GaAs substrate layers compared to that under the gate and source.

The plots in figure 22 when compared to figure 21 show that as the gate bias is reduced from 0.2V to 0V the electron concentration normal to the drain and source contacts do not change in any significant way. This is because the high doping in the AlGaAs layer makes the extent of depletion layer around the gate significantly smaller than the separation between the gate and the drain or source contacts. However, the charge distribution under the gate is modified as can be seen in the increased penetration of the depletion region in the AlGaAs layer. The electron density reaches a maximum of $1.5x10^{17}$ cm^{-3} near the AlGaAs/InGaAs interface down from $4x10^{17}$ cm^{-3} for the gate bias of 0.2V. Similarly the maximum density in the InGaAs channel reaches $4x10^{17}$ cm^{-3} near the AlGaAs/InGaAs interface down from $1x10^{18}$ cm^{-3}. Within the rest of InGaAs channel, the charge distribution is not affected by the change of the bias. Further, the density of electrons in the GaAs substrate increases by a very small amount. Since the electron density in the substrate layer is about two orders of magnitude smaller than that in both the channel layer and the AlGaAs layer near the heterojunction, its effect on the drain current in negligible. From figure 20 we see the ratio of the drain current for gate bias of 0.2V ($I_d(0.2)$) to that at 0.0V ($I_d(0)$) is given by:

$$I_d\ (0)/I_d\ (0.2) = 2.02/4.70 = 0.43$$

Similarly the ratios for electron density in the AlGaAs and channel layers are:

$$n_{AlGaAs}(0)/n_{AlGaAs}(0.2) = 1.5x10^{17}/4.x10^{17} = 0.375$$

and:

$$n_s(0)/n_s(0.2) = 4x10^{17}/1.x10^{18} = 0.4$$

This shows that the decrease in the drain current is primarily due to the reduction in the free electron density below the gate that contribute to current flow. An additional factor which is not accounted for in this study, is the fact that at zero bias more current is carried by the bulk electrons farther away form the AlGaAs/InGaAs interface. These electrons exhibit lower mobilities compared to the 2DEG at the interface. More accurate evaluation of the contribution of these different regions to the drain current requires development of a transport model that includes the quantization of the electron gas at the interface, degeneracy and nonequilibrium transport in regions where very high potential and density gradients exists.

An other important question to be addressed is how the electron density changes as one moves from the source to the drain. Figures 23 and 24 show this variation for gate bias voltages of 0.2V and 0V. The plot in figure 23a is along a line that is 30 nm from the contacts and shows that the electron density within the AlGaAs layer under the source and drain remain equal to the back ground doping level. The electron density drops sharply to $4x10^{17}$ cm^{-3} at the end of the gate contact closer to the source, and then gradually drops to $1.3x10^{17}$ cm^{-3} at the other end of the gate contact closer to the drain. The electron concentration then rises sharply to approximately $1x10^{18}$ cm^{-3} as one moves to the drain region. The location of the minimum near the drain end is due to the positive bias on the drain, so that relative to the drain the gate is strongly reverse biased. This steep change in electron density is compensated by a steep change in potential over this region from -0.9V on the gate to 1.0V on the drain.

The plot in figure 23b shows the electron distribution within the InGaAs channel along a line that is 1 nm from the AlGaAs/InGaAs interface. The electron density remains constant at $1.3x10^{18}$ cm^{-3} under the source and drops gradually under the gate to $8x10^{17}$ cm^{-3} followed by a steep drop to $1x10^{17}$ cm^{-3} at gate contact closer to the drain. Under the drain the density remains steady at $1x10^{18}$ cm^{-3}. This figure clearly shows that higher forward bias on the gate is required to fully utilize to excellent transport properties of the electrons in the InGaAs channel layer. The higher electron density in the channel at large forward gate bias combined with their higher velocities lead to higher drain current levels. This also explains why the transconductance of the PHEMT improves in the forward direction.

Figure 23c shows that at 7 nm from the AlGaAs/InGaAs interface (center of the channel) the electron concentration below the source and drain contacts is almost two orders of magnitude lower than the density at the interface. However, below the gate contact the density is significantly higher and reaches a maximum of $1.5x10^{17}$ cm^{-3} on the right half of the gate contact which is closer to the drain contact. This is a result of repulsive force on the electrons exerted by the Schottky barrier on the gate.

Reducing the gate bias to 0V leads to further reduction in electron density in the AlGaAs layer under the gate as can be seen in figure 24a. Similarly the charge density in the InGaAs channel near the AlGaAs/InGaAs interface is lower under the gate and falls below $1x10^{17}$ cm^{-3} on the drain side of the gate. Under the drain and source regions the electron distribution remains the same as before. Also the distribution of the electrons along the center of the channel is not affected by the change in the bias except for a minor increase on the source side of the gate. As emphasized above it is clear from these two figures that the drop in drain current as the gate bias is reduced from 0.2V to 0V is mainly due to the decrease in the electron density in the AlGaAs and InGaAs layer close to the AlGaAs/InGaAs interface under the gate contact.

We now display contour and projections of the potential and charge distributions within the PHEMT. In doing so we point out that the important changes in electron and potential distribution inside the PHEMT occur over the top 80-100 nm portion of the device. Indeed, the thickness of the AlGaAs layer plus the InGaAs channel where most of the current transport takes place is only 53 nm. Consequently we display the potential and electron density profiles only for the top 80 nm of the device. Furthermore, we have adjusted the scales so as to show the details of the variation in the direction normal to the contacts. Figures 25a and 25b are color contour plots of the potential for a gate bias of 0.2V and drain bias of 1.0V. The solid color plots in figure 25a show that the gate divides the device into two main regions, (1) the region below the drain (pink color) where the potential is almost flat and equal to 1.0V, (2) the region above the source where the potential is almost flat and equal to zero. Additionally, it shows that the highest potential gradients in AlGaAs occurs between the drain and the gate contacts. Similarly high potential gradients exist normal to the gate and between the gate and source, where the potential increases from -0.7 at the gate to zero on the source and bulk GaAs. The figure also shows that within the InGaAs channel, the highest potential gradients occur between the gate and drain contacts. The color contour lines in figure 25b show the highest density of potential gradients between the gate and drain. Additionally, it shows that within the channel the electric field is parallel to the heterojunction interface and is strongest on the drain side of the gate contact.

The electron distribution for the same bias conditions are shown in figures 26a and 26b. The solid color plot in figure 24a shows that under the drain and source contacts the electron concentration in the AlGaAs layer is equal to the background doping level ($1x10^{18}$ cm^{-3}). It also shows the strong depletion under the gate. Within the InGaAs channel, the maximum concentration occurs near the AlGaAs/InGaAs interface and decreases rapidly as one moves away from the interface. The density in the channel away from the interface under the drain is higher than under the source. However the maximum concentration occurs under the gate. Within the GaAs substrate, the concentration is highest under the drain and decreases gradually to a minimum under the source. Note that the highest concentration in the GaAs substrate layer near the InGaAs/GaAs interface occurs at the region intermediate between the gate and drain contacts. This is because the electrons as they pass under the gate are subjected to a repulsive force that pushes them away from the AlGaAs/InGaAs interface to GaAs substrate. As a result some electrons have a

large momentum component normal to the interface after passing under the gate and are able to cross the potential barrier at the InGaAs/GaAs interface. The three dimensional plot in figure 27 shows clearly the build up of the electron density at the InGaAs/AlGaAs interface, the complete depletion under the gate, and the drop in electron density in AlGaAs layer close ot the heterojunction. Additionally, it shows that within the InGaAs channel a sharp drop in the electron concentration under the source occurs as one moves away from the interface. It also shows how the presence of the potential barrier at the InGaAs/GaAs leads to an other sharp drop in the density as one moves away from the interface into the GaAs substrate. Within the GaAs layer the electron concentration increases as one moves to the regions below the gate and drain.

5.2.3. Modifications in the Design of the PHEMT

The role played by the potential barrier at InGaAs/GaAs interface under the source and the drain provides an interesting insight to the performance of the PHEMT. Whereas it reduces the electron concentration by two to three orders of magnitude under the source and gate, it only reduces it by a factor of three under the drain. This raises the possibilities of obtaining better performance by raising the height of the potential barrier at the InGaAs/GaAs interface. The increased barrier height will decrease the fraction of electrons that escape to the GaAs substrate under the drain and gate leading to higher current densities and faster switching. Fortunately, increasing the barrier height is possible only through increasing the mole fraction of in the InGaAs which leads to better velocity-field characteristics. This increased velocity of the electrons in the InGaAs channel will definitely lead to faster switching of the PHEMT devices. However, the experimental difficulties in growing InGaAs layers with large In mole fraction (x>50%) on GaAs substrates due to excessive strain sets an upper limit on the improvement of the device performance by changing the channel composition. Fortunately, even using only InGaAs with In mole fraction between 30% and 40% will likely double the height of the potential barrier at the InGaAs/GaAs interface. Consequently, the fraction of electrons that escape to the GaAs substrate will be significantly reduced which results in better electrical characteristics. An alternative approach to use InGaAs channel with In mole fraction greater than 50% is to use InP substrates instead of GaAs because lattice matching is accomplished at 53% In mole fraction. The poor quality of the InP substrate and the presence of large concentrations of unwanted n-type impurities in the grown eptaxial layers cause parasitic conduction in the device. These difficulties are expected to be overcome as the technology improves and more experience in device fabrication is achieved.

5.2.4 Transient Response:

The electro-optic sampling approach measures the response of the solid state devices by perturbing the gate by a voltage pulse with a finite rise time. The shape and duration of the pulse are determined by the properties of the semi-insulating GaAs photoconductor connected to the gate contact as well as the duration and power of the pump laser pulse that excites the electron-hole pairs in the photoconductor (see figure 1). The response of the device is then monitored by a probe pulse that is incident on an electro-optic material and records the change in the properties of the material as a result of the

change in the drain current. Thus apart form the complexity of the experimental setup, one can simulate this measurement procedure by numerical solution of the equations governing the transport of electrons inside the PHEMT using a transient accurate algorithm.

In the transient simulation the time evolution of the drain current is calculated for a time dependent bias on the gate. The initial state of the device corresponds to the steady state under a set of drain and gate bias voltages. The gate is then perturbed with a voltage pulse of predetermined shape and duration. The perturbing voltage pulses used in this simulation are shown in figure 28. These shapes were selected to determine whether the response of the device is dependent on the pulse rise time, duration and shape.

When the gate is perturbed by the first voltage pulse, the bias changes instantaneously (zero rise time) from 0V to 0.2V and stays at 0.2V for 1.0 picosecond and drops back to 0V with zero fall time. The drain current becomes negative immediately and reaches -100 in units of reference current within the first 20 femtosecond and then rises back to positive 10 units at 1 picosecond as can be seen in figure 29a. When the gate bias switches back to 0V after 1 picosecond, the drain current rises to 86 units within 50 fs of the switching event. The drain current then drops back to 8 units one picosecond after the switching of the gate bias to 0V. This rapid drop is followed by a slow relaxation of the drain current to within 4% of th steady state current for this set of bias conditions after 10 picoseconds from switching the gate bias to 0V as shown in figure 29b. This clearly shows us that there are two components in the response of the device. A fast component that lasts for one to two picoseconds and a slow component that lasts for about 10-12 picoseconds. The question is then what can this transient response tell us about the speed of the device. In other words is it enough to measure the 10% to 90% rise time of drain current to get an estimate of the speed of the device. This approach has been adopted by the group at the University of Rochester as a means of measuring the speed of the HEMT and PBT. Unfortunately, this does not give an absolute measure of the speed of the device. For example, the steady state drain currents for the PHEMT are 8.4 and 19.6 units for gate biases of 0V and 0.2V, respectively. However, after one picosecond of switching the gate bias from 0V to 0.2V, the drain current reaches only 10 units which is about 50% of the steady state current. Accordingly the speed of the PHEMT is greater than one picosecond. On the other hand, one picosecond after switching the gate bias back to zero the drain current reaches 9.4 units which is only 12% above the steady state current and falls below 10% five picoseconds later. This asymmetry in the response raises some doubts about taking the response as a measure of the speed of the device. Instead a proper definition of speed should be

> "the time it takes the device response to fall within 5%-10% of its steady state response corresponding those bias conditions".

Applying this criterion to the PHEMT shows that it takes the drain current 7 picoseconds to fall within 5% of steady state current for a zero gate bias. Thus the speed of response of the PHEMT is 7 ps.

However, in an experiment the perturbing voltage pulses have finite rise times. Therefore although the above calculation demonstrates the problems associated with taking the device response as a measure of device speed, it does not simulate experimental conditions where the pulses have finite rise times. Because of the limited time and the nature of Phase I SBIR, we have used pulses with one and two picosecond durations and very small rise times. The dashed curve in figure 30 corresponds to the situation where the time dependent voltage pulse superimposed on the gate takes the following form:

$$Vg(t) = 0.2[1.0 - \exp(-t/t_r)]$$

the RC rise time of the pulse t_r is taken to be 0.25 ps. Thus after one picosecond the gate is practically forward biased by a 0.2V after being switched form an initial steady state corresponding to zero gate bias. Comparing the response in this situation to that in figure 27a, we find that the drain current reaches the maximum negative value after 0.1 picosecond and rises gradually to reach a maximum of 21 units after 8 picoseconds which is 8% above the steady state current. The current stays at the same level up to 10 ps and should take longer to relax to within 5% of the steady state current. Thus we see that although it took only 7 ps for drain current to be within 5% of the steady state value in figure 27a, it takes more than 10 ps to reach the same level when the pulse has a finite rise time and the final steady state gate bias is different from the initial one.

Next the gate was perturbed with a gaussian voltage pulse centered at 0.5 ps and with a standard deviation of 0.25 ps. The solid curve in figure 30 shows the time dependence of the drain current for this situation. Note that the response is symmetric in this case and reaches a maximum negative value of 70 units 0.4 ps after the onset of the pulse. The drain current then rises rapidly to reach a positive maximum 0.3 ps later. This shows that the direction of the drain current response is very sensitive to the shape of the pulse and where the rising and falling edges in the pulse occur. The current then drops rapidly and reaches a value of 8.7 units which is within 5% of the steady state current two picoseconds after the pulse onset. The drain current slowly relaxes to within 2% after 8 picoseconds. In this situation the device returns to its initial state very rapidly as can be inferred from the return of the drain current to within 5% of the steady state current in two picoseconds. However, this does not mean that the speed of the PHEMT is two picoseconds because the transient intermediate states did not have sufficient time to develop to well defined states. Thus the deviation from the initial states might have been very marginal. In a real world environment, the devices are switched between well defined bias points, such that the potential rises over a finite time from one level to an other where it remains constant for a finite time in a way that resembles the second situation discussed in the previous paragraph.

The calculation was then repeated with gaussian voltage pulses with standard deviation of 0.5 ps and centered at 1 ps from the onset of the pulse for initial gate biases of -0.2V and 0V. The two curves in in figure 31 are the plots of the drain current for these two bias conditions. Both curves are almost symmetric about 1 ps where the pulse is centered and have the same shapes apart from being shifted with respect to each other. At all times the

drain current for the initial gate bias of 0V is higher than the one with -0.2V bias. This is in qualitative agreement with the response of the HEMT shown in figure 1b which was measured using the picosecond electro-optic sampling technique. The electrical pulse used in the measurement was generated using a GaAs photoconductor and had a rise time of 5 ps and much longer duration than pulses used in the simulation. Consequently, the response of the device shows a much longer rise time compared to simulated results with the gaussian pulses which show a rise time of less than a picosecond.

The above calculations show that the rise time of the response of the PHEMT is strongly dependent on the shape, duration and rise times of the perturbing pulses. Additionally, very short and symmetric pulses show a symmetric response about the center of the pulse. With these short pulses the device tends to return back to its initial state quickly indicating that the intermediate states during the pulse were not far removed from the initial state. More work is needed to understand the nature of these intermediate states and the optimum pulse width and duration required to get an estimate of the rise times of the response of these devices.

6. SUMMARY AND CONCLUSIONS

The present study has demonstrated that numerical simulation can be used effectively as a tool to assess the operating principles of the vertical HEMT, the pseudomorphic HEMT and whether experimental measurements using the electro-optic subpicosecond sampling provide the means to estimate the speed of these devices. The major conclusions of this study are:

1. The VHEMT structure examined in this study requires a very high reverse bias on the gate to pinch of the channel and has a maximum transconductance of 94 mS/mm at a drain bias of 2.0. This is a consequence of the lightly doped ($N=3x10^{16}$ cm^{-3}) GaAs layer at the center of the device, which provides a low resistance current path under reverse bias conditions. We recommend that future designs keep this region undoped so as to maintain the bulk of current flow close to heterointerface and within the highly doped AlGaAs layer.

2. The undoped layer between the N^+ drain region and the highly doped AlGaAs layer is always flooded with electrons from both sides and the presence of heterointerface confines a significant number of electrons near the interface. Reducing the thickness of this layer will increase the electron concentration in this layer which will then provide a lower resistance and shorter path for the electron current. Additionally, the

   effect of the drain bias on the electrons in this layer will be stronger due to reduced distance between the drain contact and the heterointerface.

3. The PHEMT structure investigated in this study exhibit high current levels and transconductances comparable to the experimental results. The maximum transconductance in the forward direction is 375 mS/mm at a drain bias of 3.0V. However, in the reverse direction the maximum transconductance is 188 mS/mm.

4. The presence of the potential barrier at the InGaAs/GaAs interface reduces the fraction of electrons that escape to the GaAs substrate. This effect is more significant under the source compared to under the drain and gate. This reduces the length of the path the electrons follow from the source to drain resulting in high current levels and faster switching properties. Additionally, within the InGaAs channel the confinement of electrons near the AlGaAs/InGaAs is largest under the source than under the gate or drain.

5. The performance of the PHEMT can be improved by increasing the mole fraction of Indium in the InGaAs channel. This will increase the potential barrier height at the InGaAs/GaAs interface which will further reduce the fraction of electrons that diffusive to the undoped GaAs substrate in addition to improving the velocity/field characteristics of the electrons.

6. The transient response of the PHEMT is strongly dependent on the shape and duration of the perturbing voltage pulse superimposed on the gate. The response is symmetric about the center of the perturbing symmetric pulses. A good measure of speed is the time it takes the device to reach the steady state response corresponding to that set of bias conditions.

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MATERIAL	μ_0 ($cm^2/V \cdot s$)	a (cm/s)	b (cm/s)	c (cm/s)	F_v (V/cm)
GaAs	7500	1.0×10^6	6.0×10^6	7.5×10^6	3.5×10^3
$Al_{.15}Ga_{.85}As$	4800	-1.45231×10^6	3.42348×10^6	7.0×10^6	3.5×10^3
$In_{.15}Ga_{.85}As$	8850	-5.05572×10^6	1.27384×10^7	7.5×10^6	3.5×10^3

TABLE 1. Velocity-Field Curve Parameters used throughout this Study.

Table 2: Material Parameters

	GaAs	$In_{.15}Ga_{.85}As$	$Al_{.15}Ga_{.85}As$	$Al_{0.2}Ga_{0.8}As$
m^*_n	0.067	0.061	0.0795	0.0836
$N_c\ (cm^{-3})$	4.34×10^{17}	3.77×10^{17}	5.60×10^{17}	6.04×10^{17}
m^*_p	0.48	0.47	0.527	0.542
$N_v\ (cm^{-3})$	8.31×10^{18}	8.06×10^{18}	9.56×10^{18}	9.98×10^{18}
E_g (eV)	1.43	1.27	1.618	1.674
$n_i\ (cm^{-3})$	1.79×10^{6}	3.72×10^{7}	5.87×10^{4}	2.11×10^{4}
χ (eV)	4.07	4.18	3.95	3.858

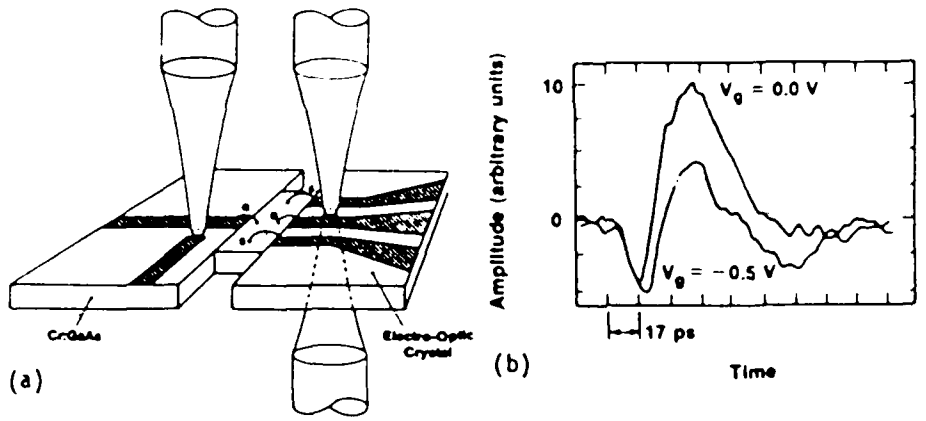

Figure 1. (a) The coplanar sampling geometry used for characterizing a MODFET. The transistor is sandwiched between a GaAs photoconductive detector used to trigger the gate and a coplanar lithium tantalate modulator for sampling the current pulse output from the drain. (b) MODFET response to a short electrical pulse produced by a GaAs photoconductive detector. The traces show the response with the gate pinched off (V_g = −0.5 V) and with the gate on (V_g = 0.0 V). The rise time with the gate on is 16 ps.

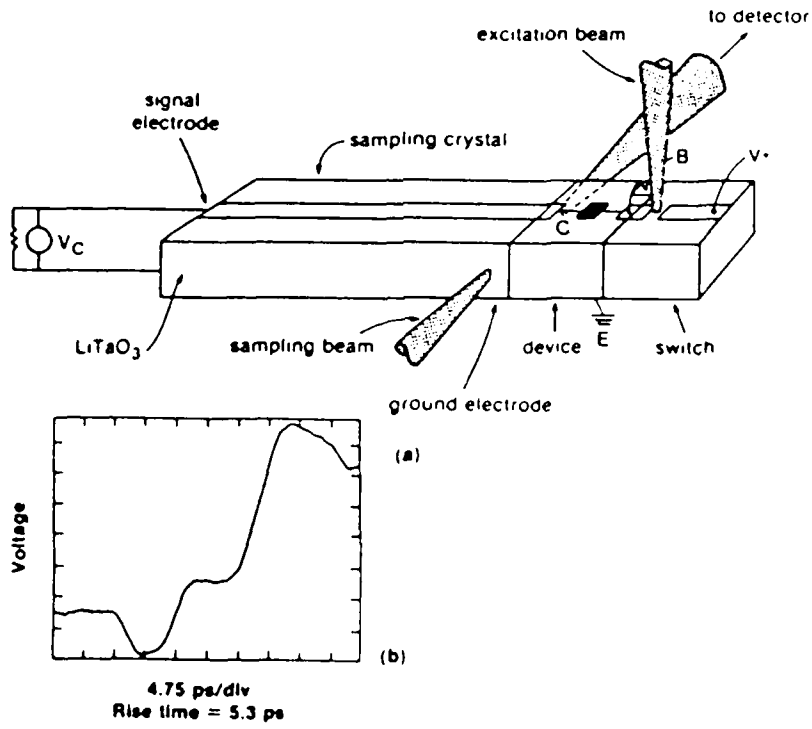

Figure 2. (a) Sampling geometry for PBT characterization. Looping wire bonds were used for bias leads to prevent loading of high-speed signal paths. (b) Step response of PBT as measured by the electro-optic sampling system.

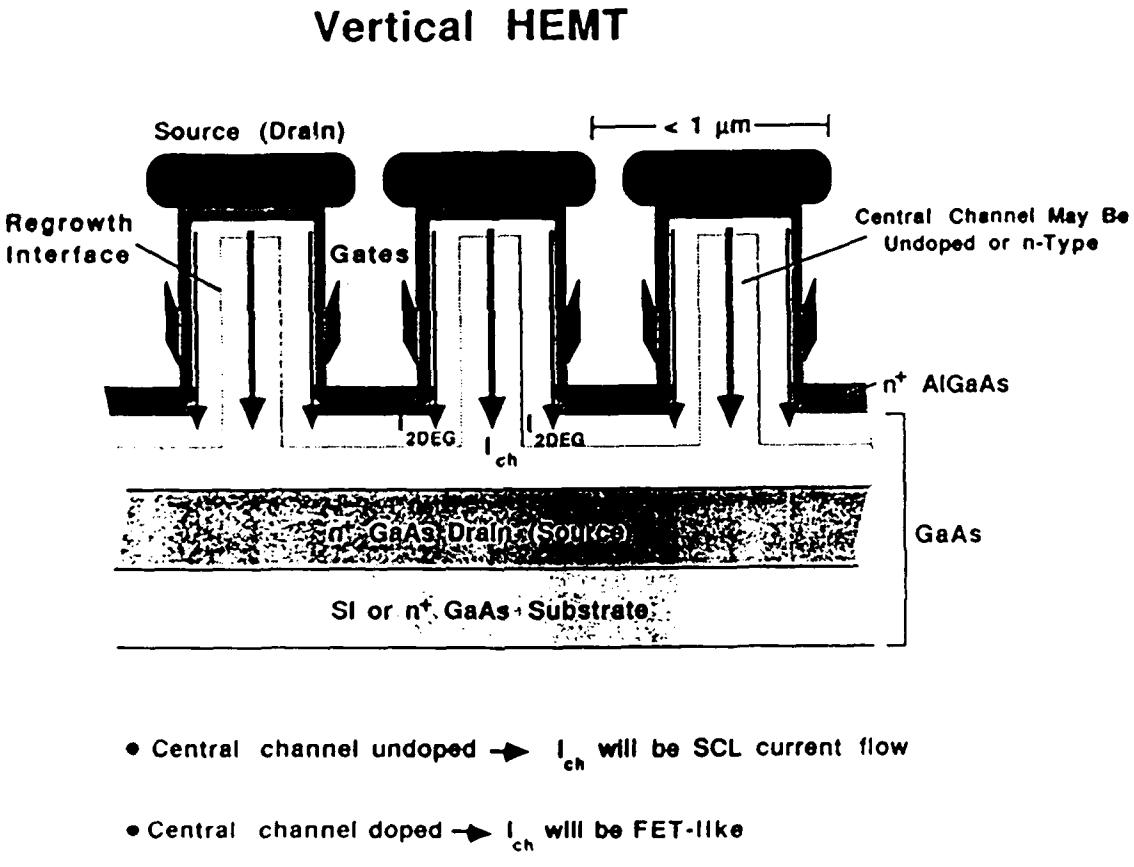

Figure 3a. Schematic of the VHEMT showing the anticipated two modes of operation.

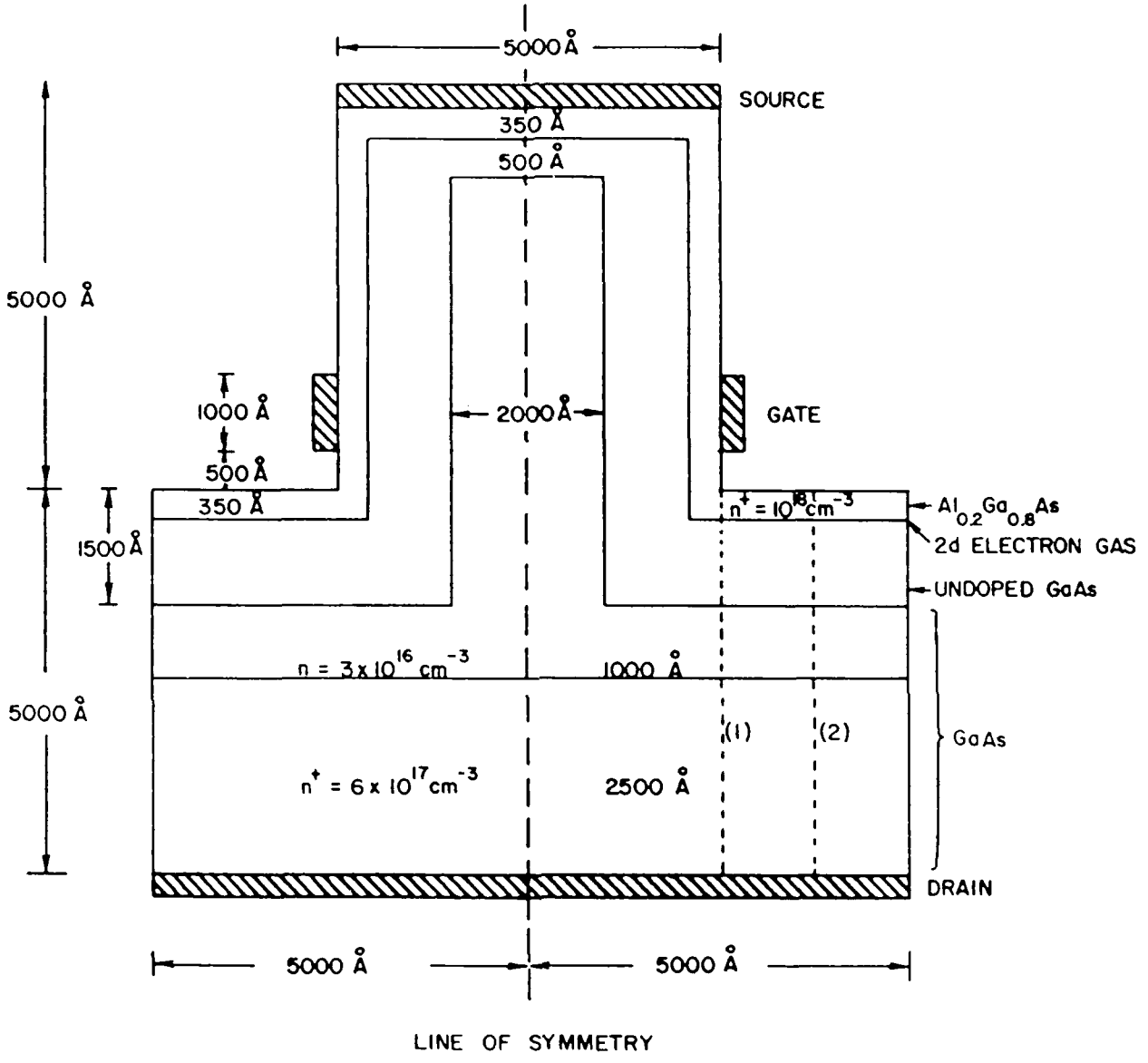

Figure 3b. Basic VHEMT unit as proposed by Lincoln Laboratory used in simulation.

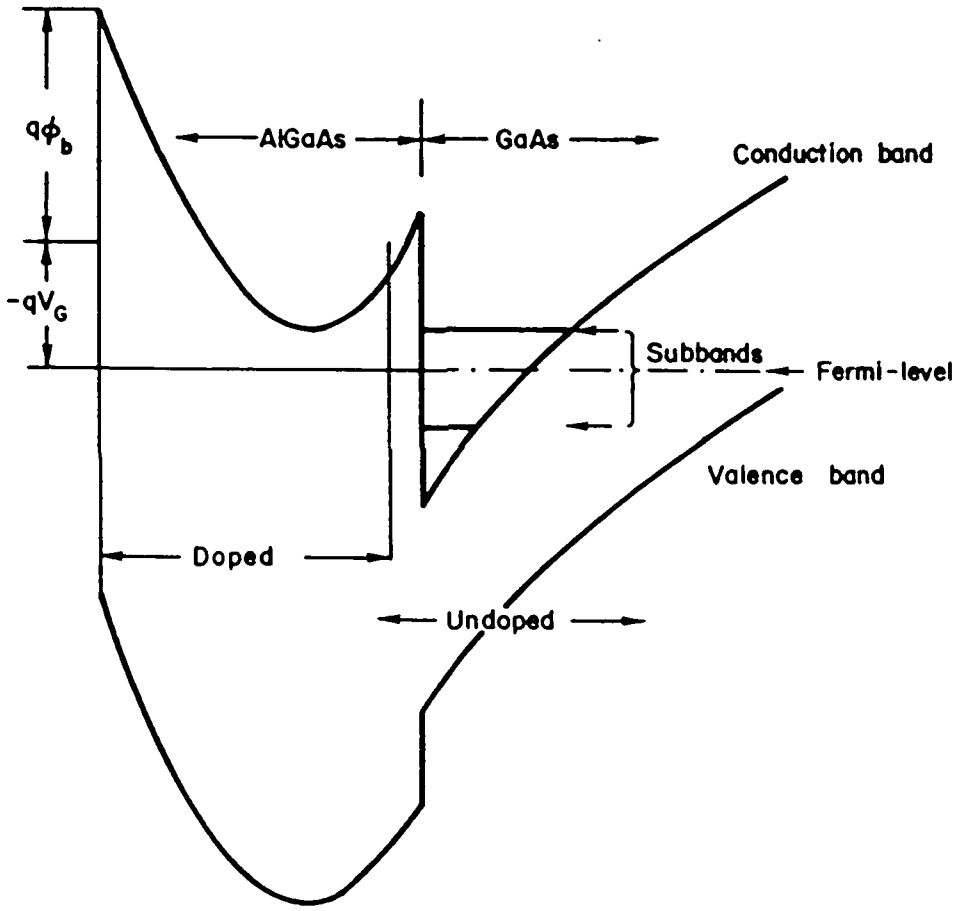

Figure 4. Energy band diagram of an $Al_xGa_{1-x}As/GaAs$ modulation doped structure with the first quantum subband filled and second subband partially filled. The depletion in $Al_xGa_{1-x}As$ near the surface is caused by the Schottky barrier gate.

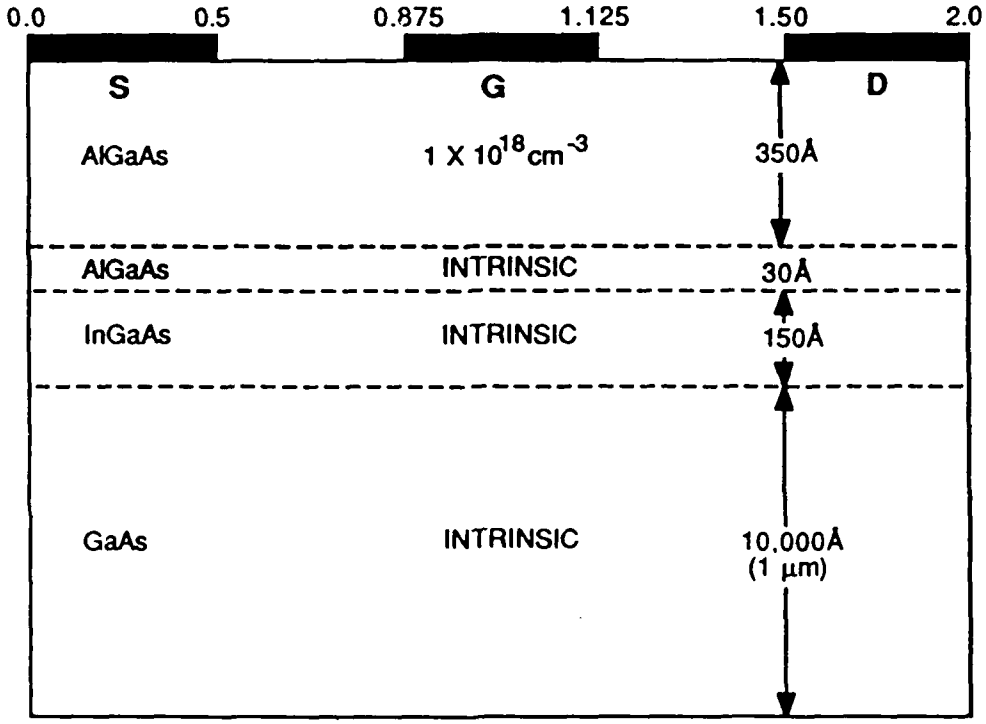

Figure 5. Schematic of the InGaAs/GaAs pseudomorphic HEMT used in this study.

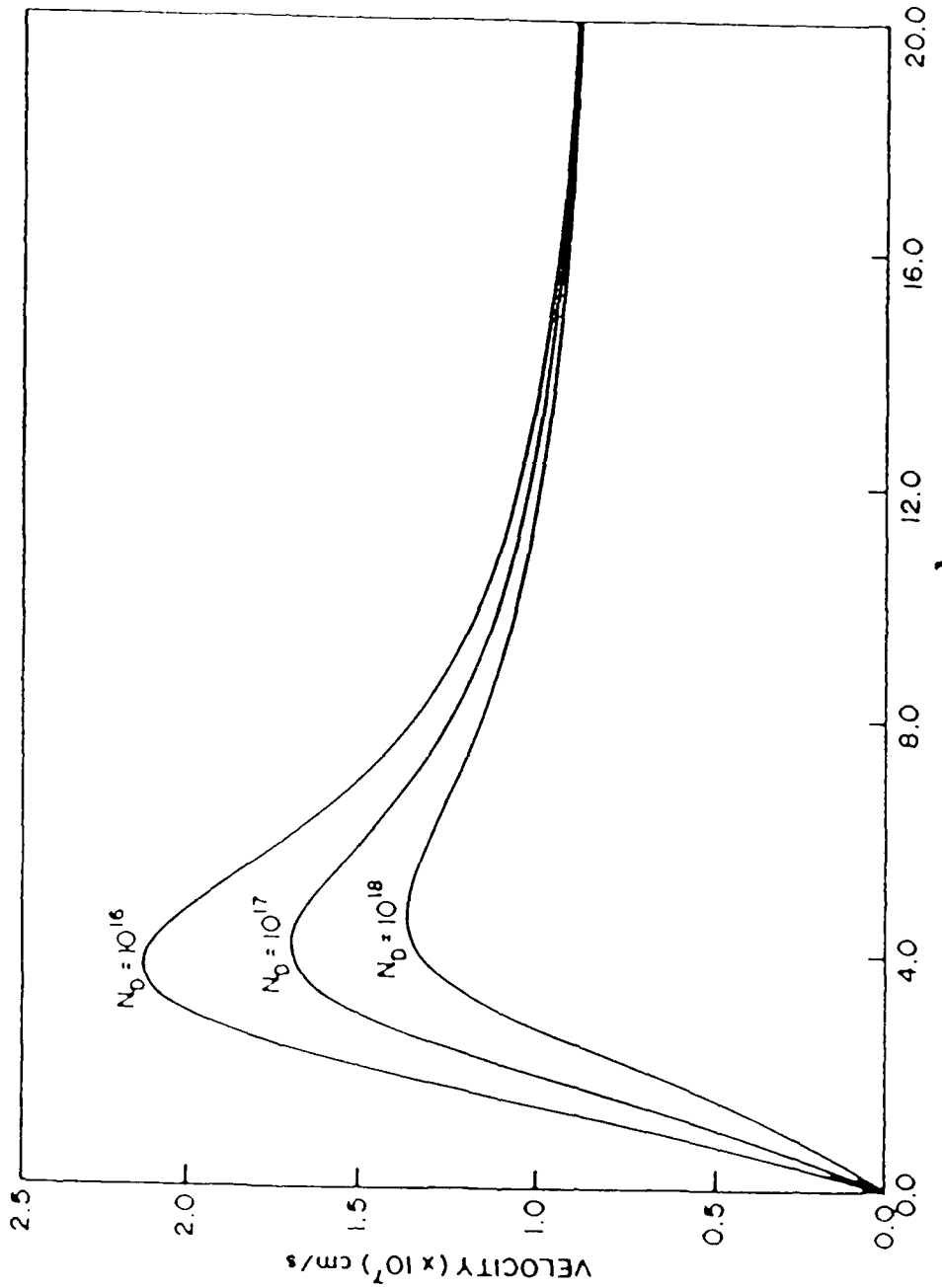

Figure 6a. Velocity field characteristics for GaAs.

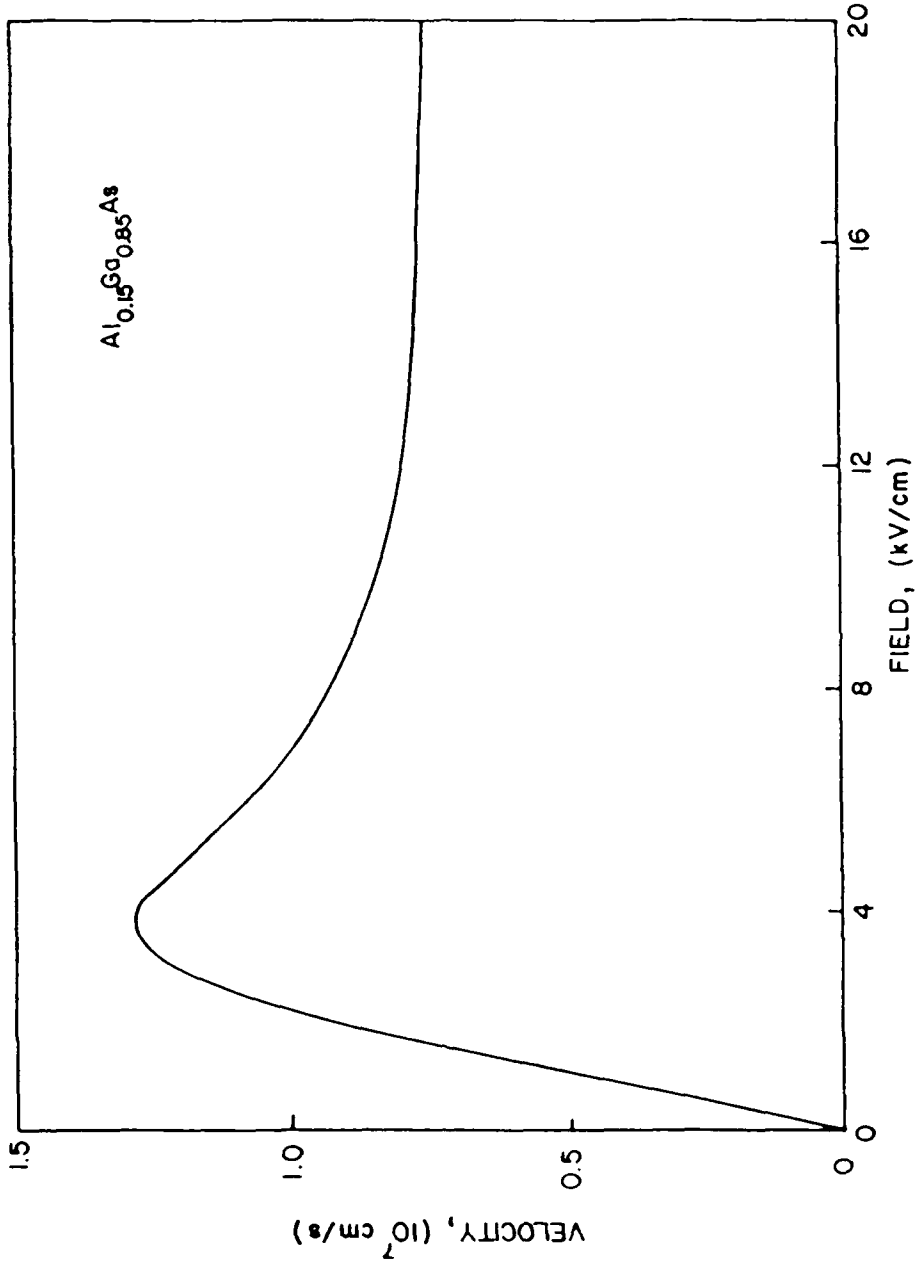

Figure 6b. Velocity field characteristics for $Al_{0.15}Ga_{0.85}As$.

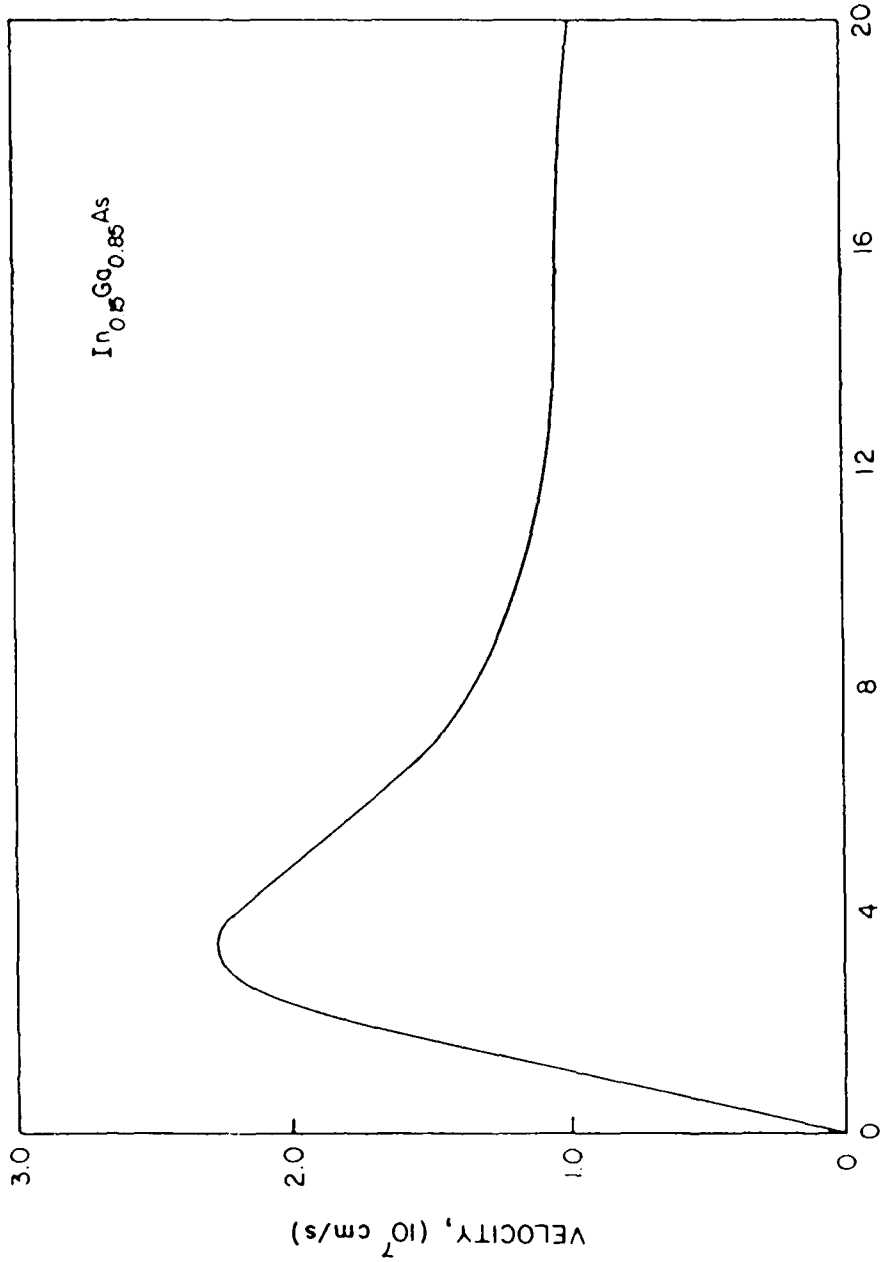

Figure 6c. Velocity field characteristics for $In_{0.15}Ga_{0.85}As$.

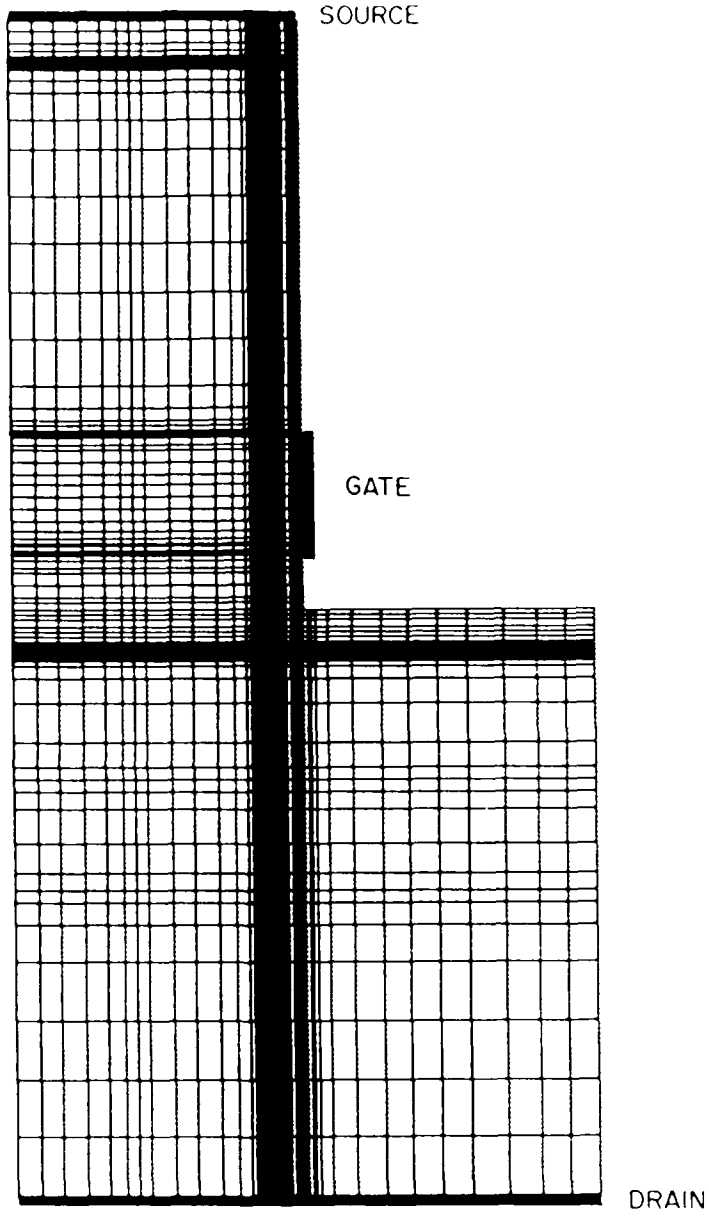

Figure 7. Grid structure used in the numerical simulation of the VHEMT.

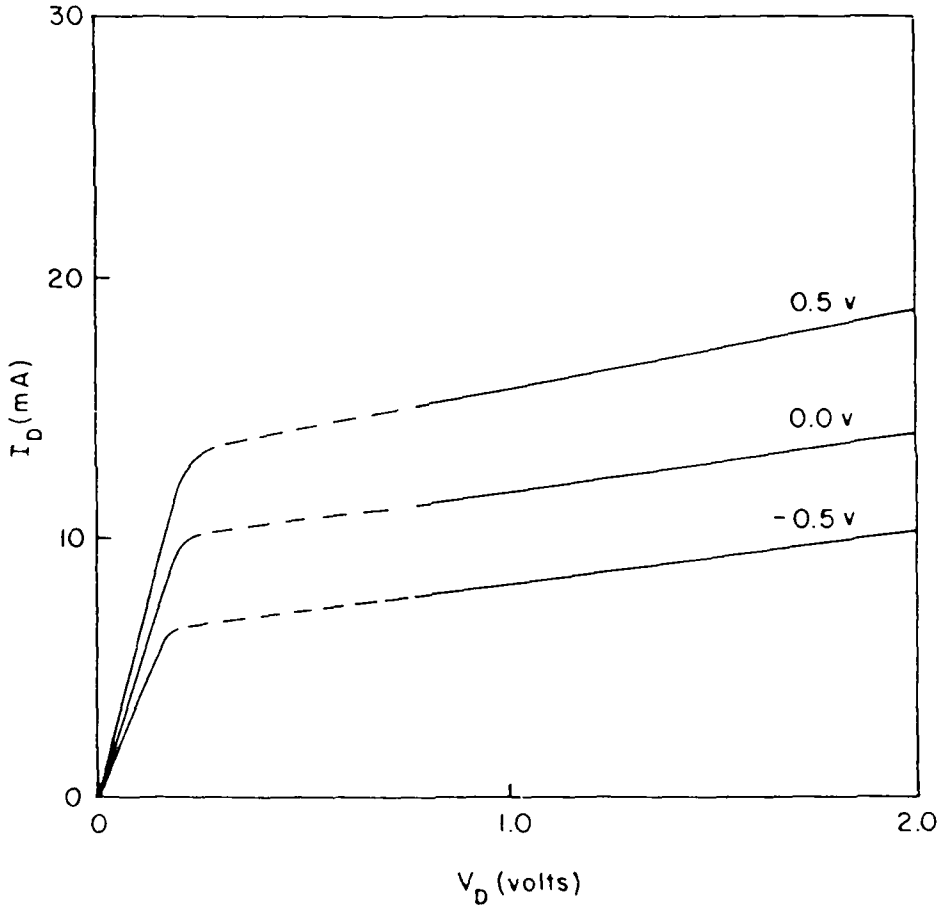

Figure 8a. Drain I-V characteristics of the VHEMT.

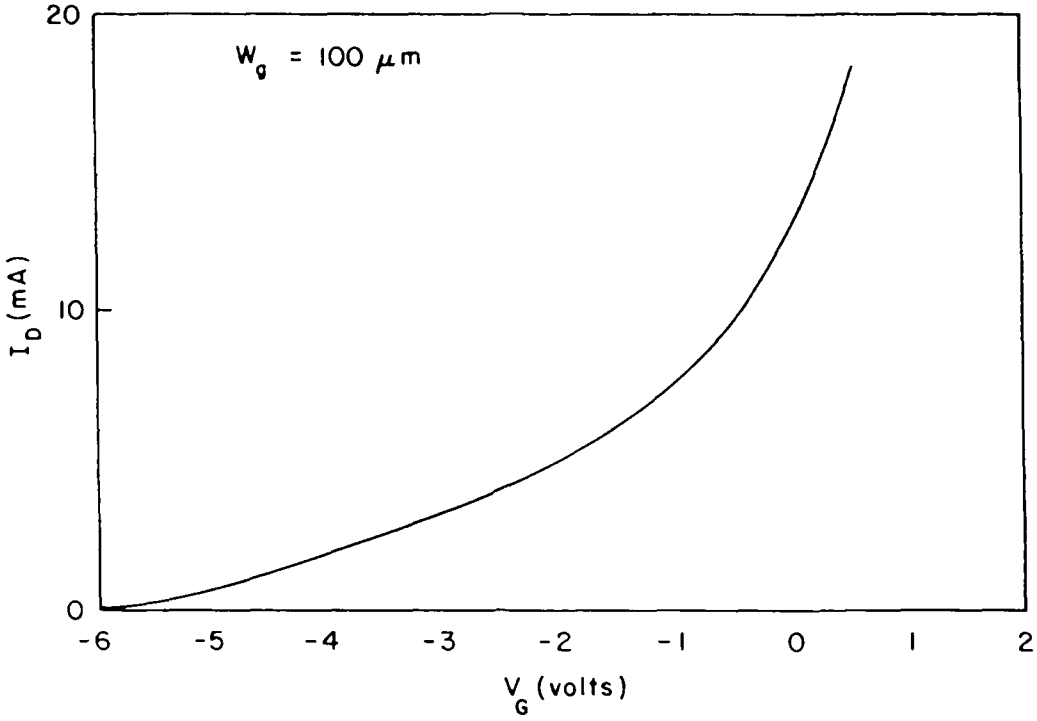

Figure 9a. Drain current vs. gate voltage for the VHEMT.

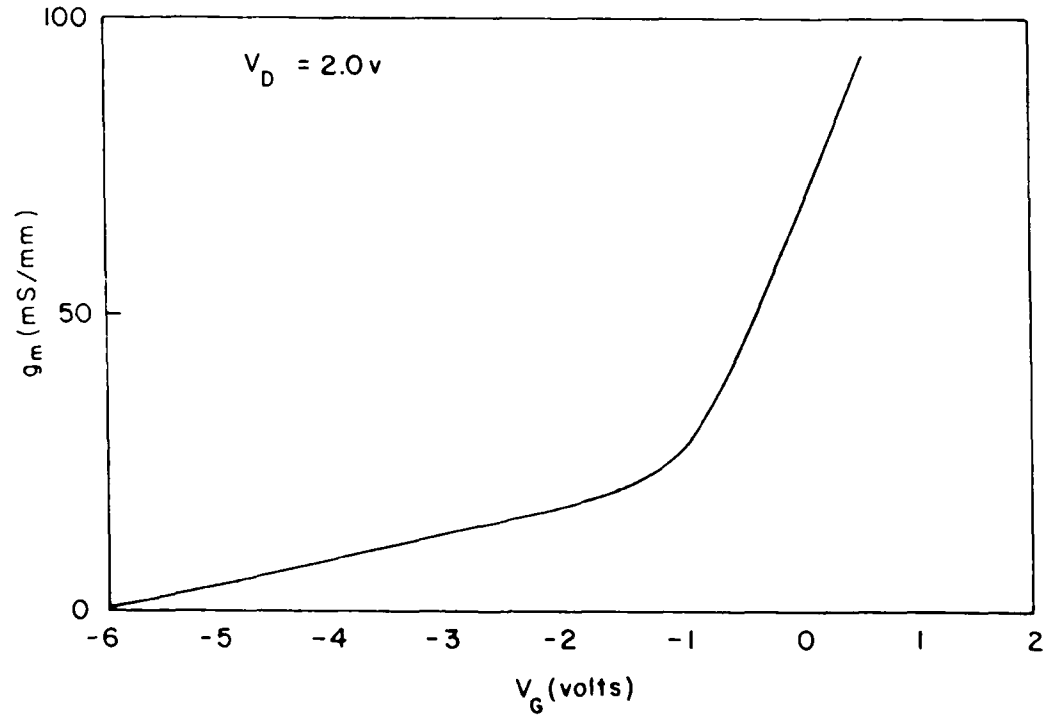

Figure 9b. Plot of the transconductance as a function of gate voltage for the VHEMT.

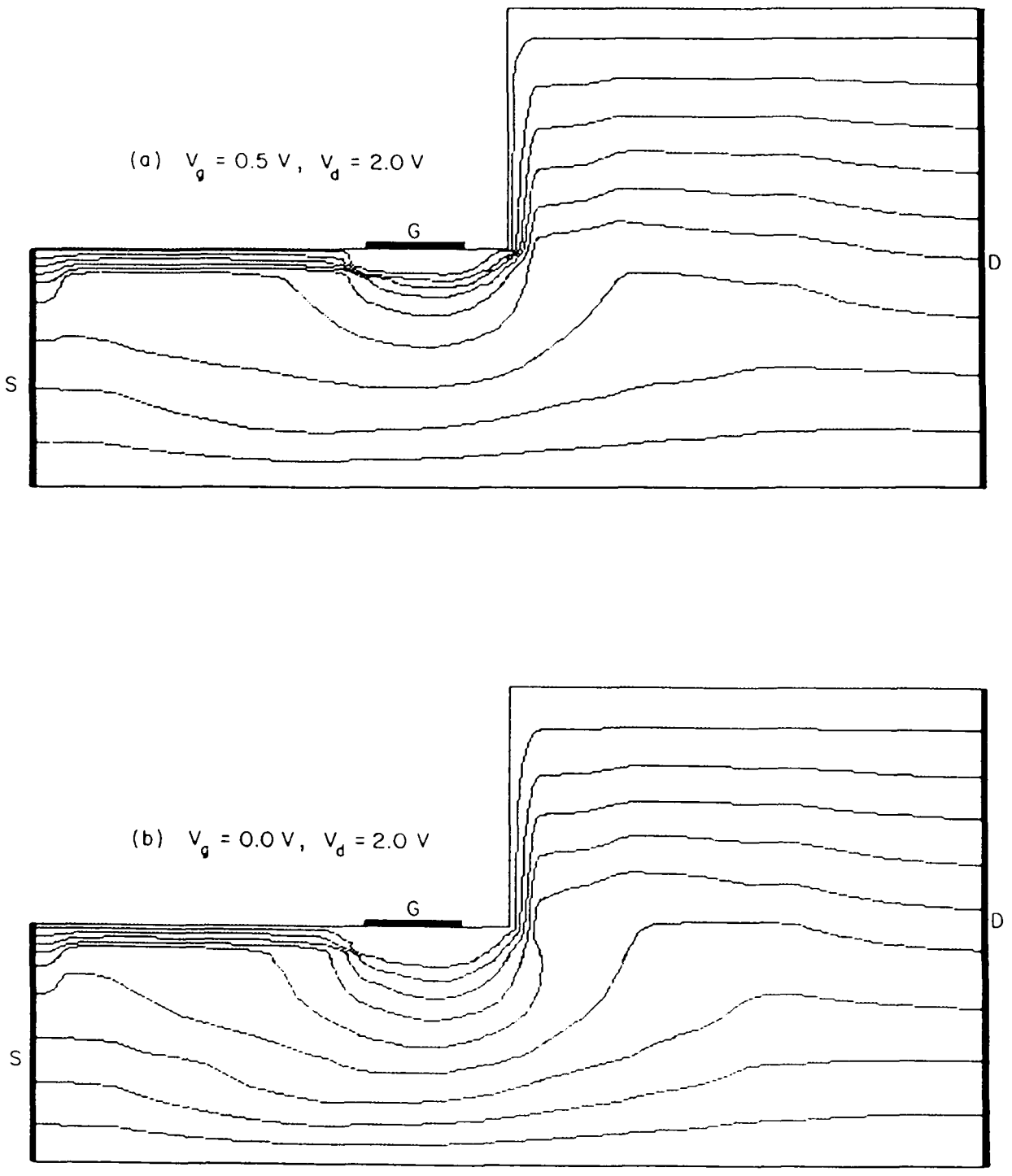

Figure 10. Current streamlines for the VHEMT at V_D = 2.0 V and (a) V_G = 0.5 V, (b) V_G = 0.0 V.

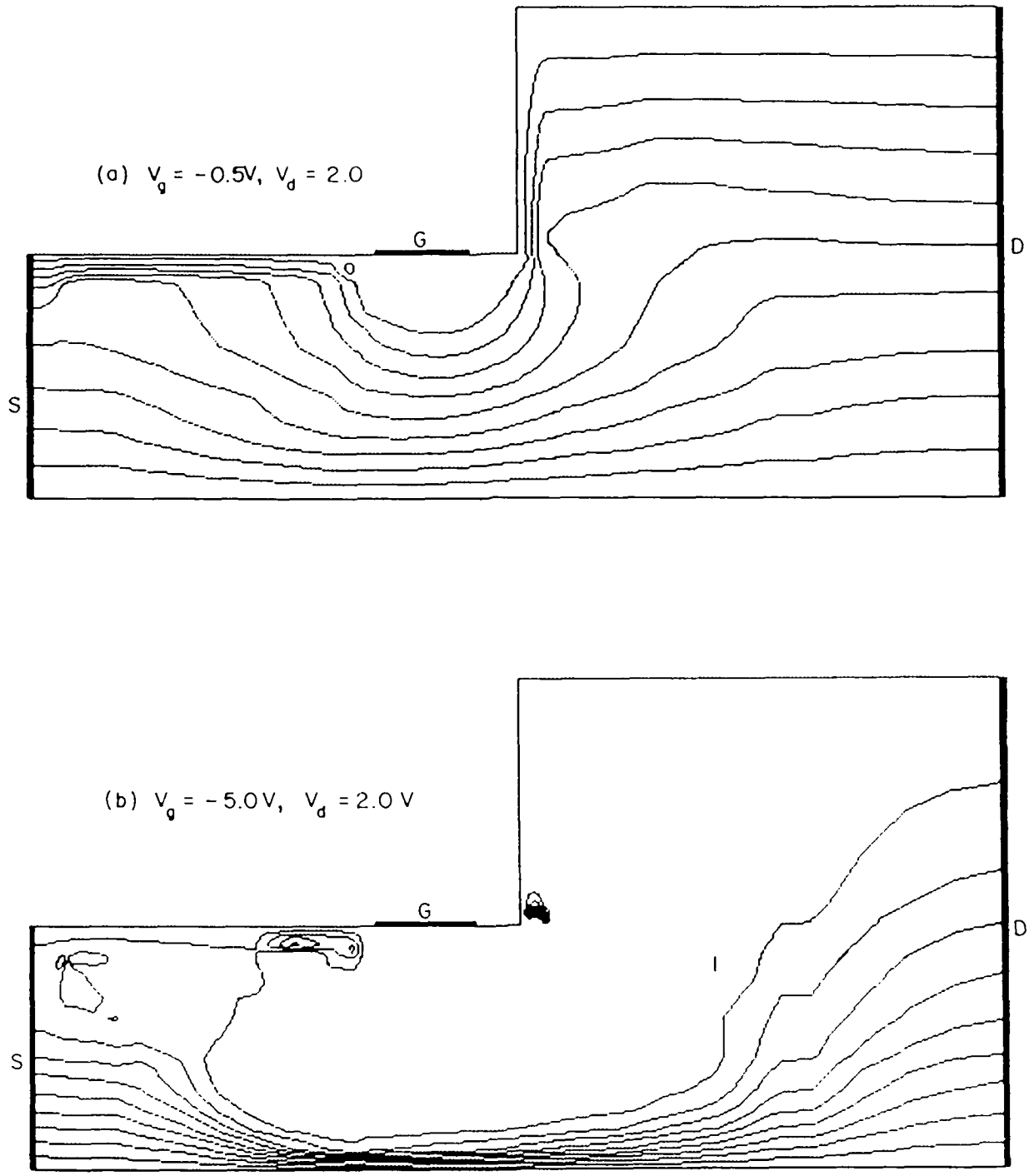

Figure 11. Current streamlines for the VHEMT at V_D = 2.0 V and (a) V_G = -0.5 V, (b) V_G = -5.0 V.

CONTOUR LEVELS

-4.250
-4.150
-4.050
-3.950
-3.850
-3.750
-3.650
-3.150
-3.050
-2.950
-2.850
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-2.350
-2.250
-2.150
-2.050
-1.950

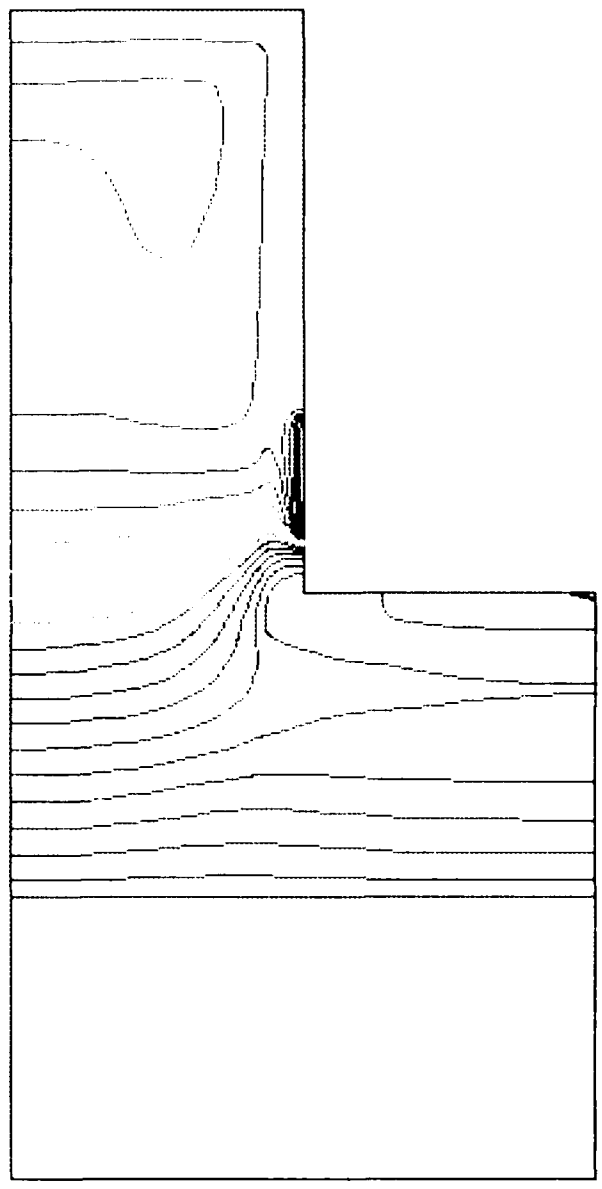

Figure 12a. Color contour plot of equipotential lines inside the VHEMT for V_D = 2.0 V and V_G = 0.5 V.

CONTOUR LEVELS

-4.250
-4.150
-4.050
-3.950
-3.850
-3.750
-3.650

-3.150
-3.050
-2.950
-2.850
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-1.950

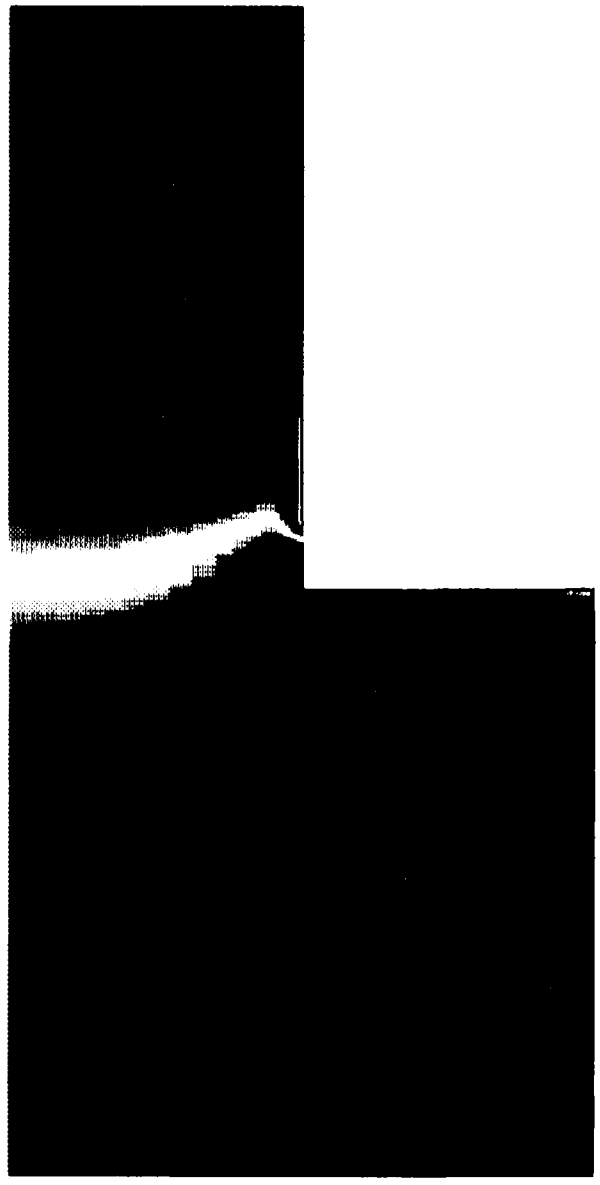


Figure 12b. Solid color plot of equipotential lines inside the VHEMT for V_D = 2.0 V and V_G = 0.5 V.

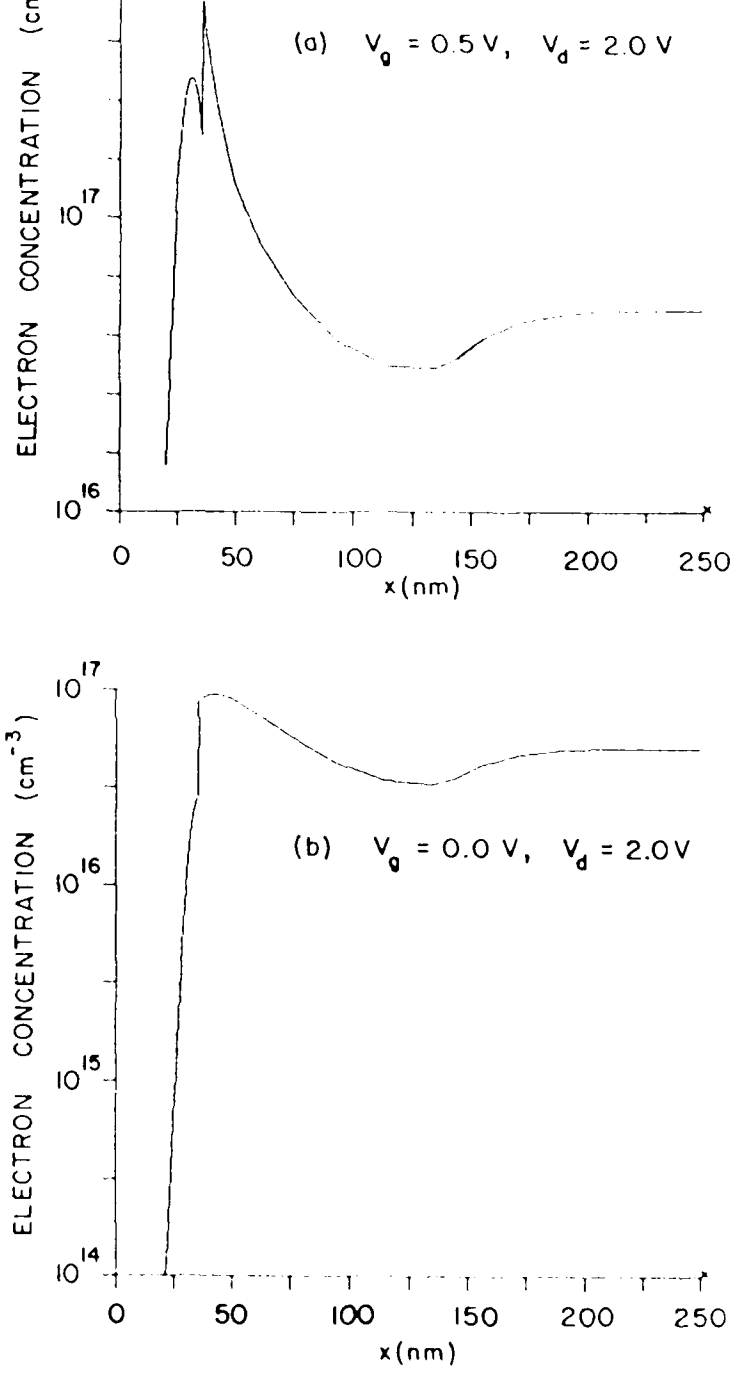


Figure 13. Variation of electron concentration along a line normal to the gate. For the VHEMT (a) V_G = 0.5 V, (b) V_G = 0.0 V.

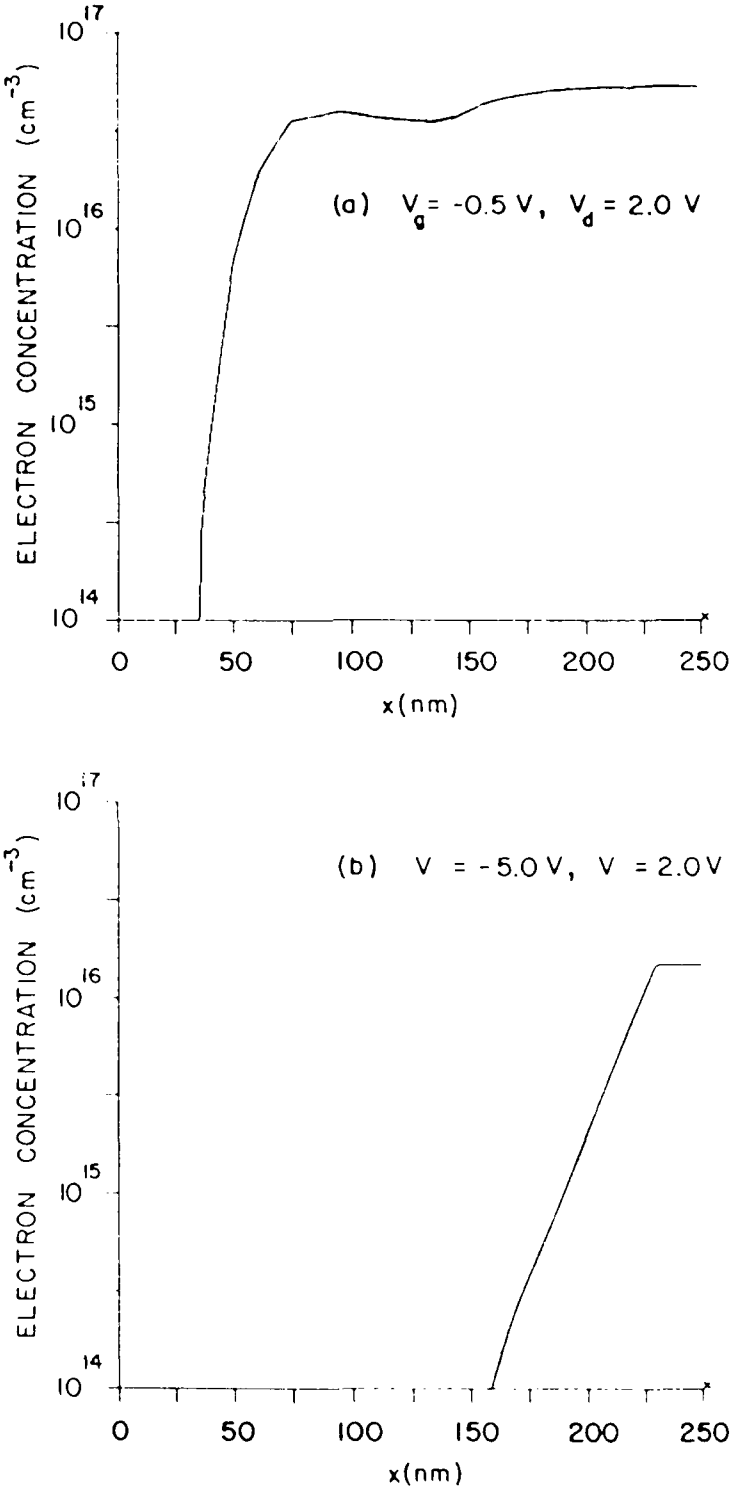


Figure 14. Variation of electron concentration along a line normal to the gate. For the VHEMT (a) V_G = -0.5 V, (b) V_G = -5.0 V.

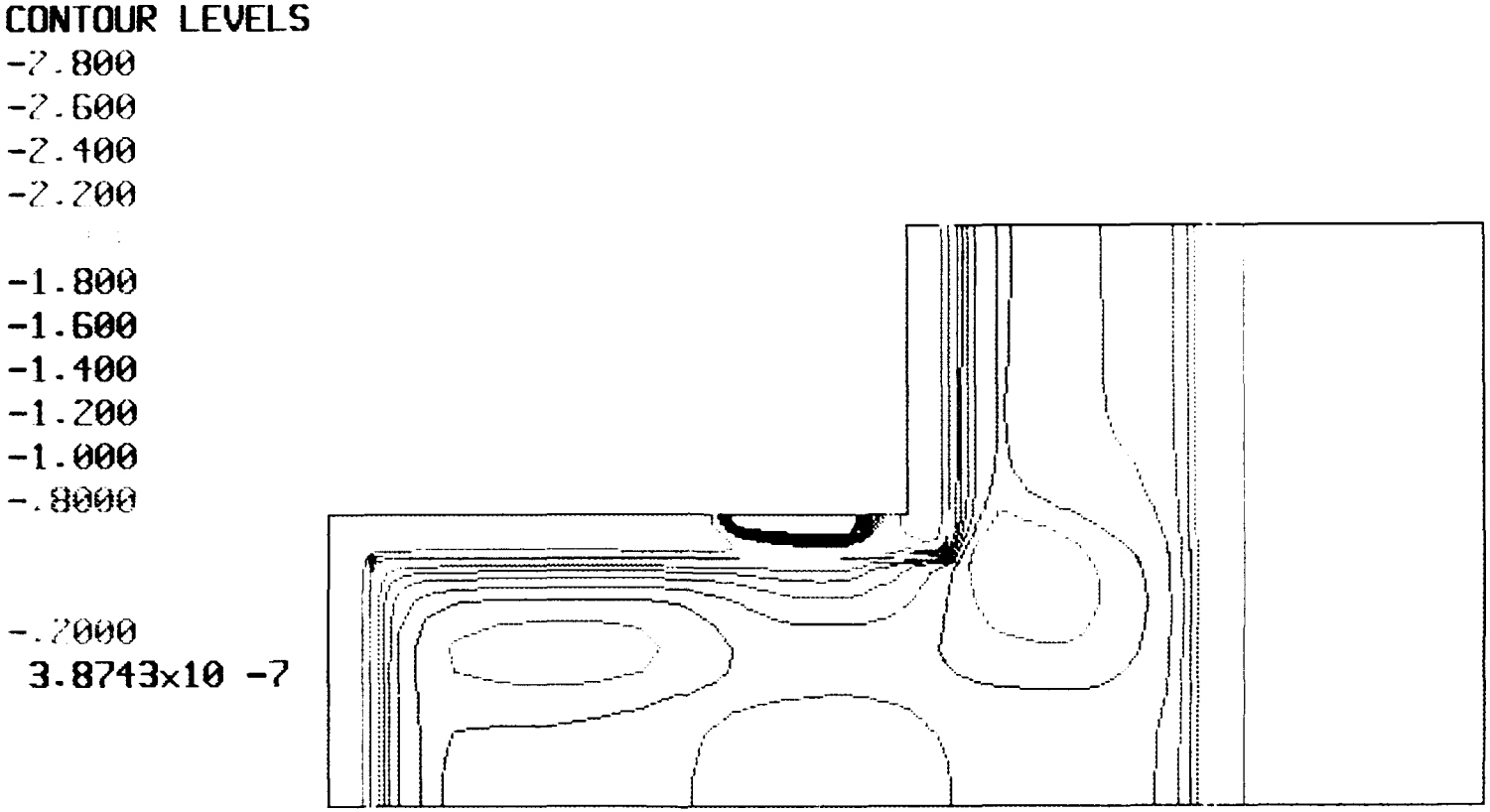


Figure 15a. Color contour plot of electron concentration on a log scale within the VHEMT for V_D = 2.0 V and V_G = 0.5 V.

Figure 15b. Solid color plot of electron concentration on a log scale within the VHEMT for V_D = 2.0 V and V_G = 0.5 V.

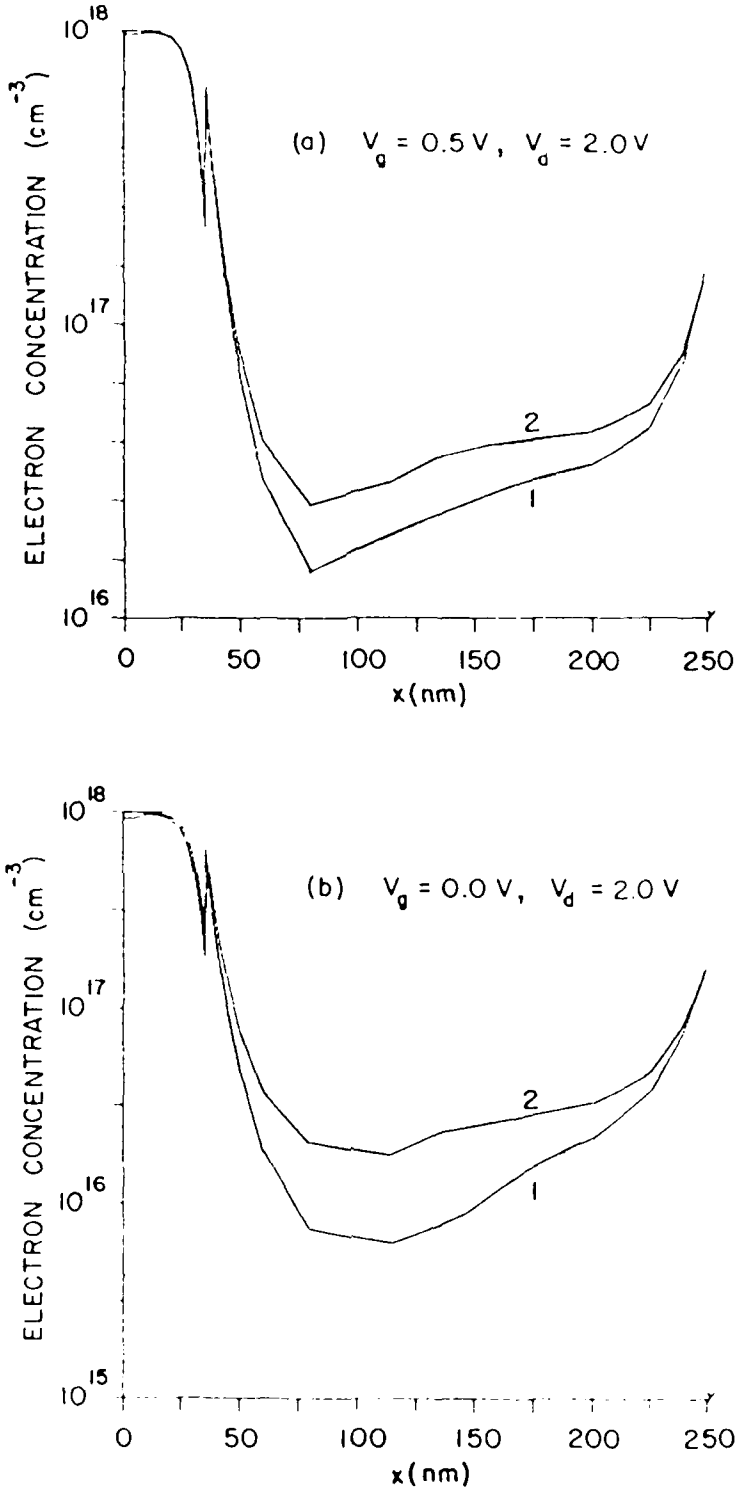


Figure 16. Variation of electron concentrations along the two lines denoted by (1) and (2) in Figure 3b for (a) V_G = 0.5 V, (b) V_G = 0.0 V.

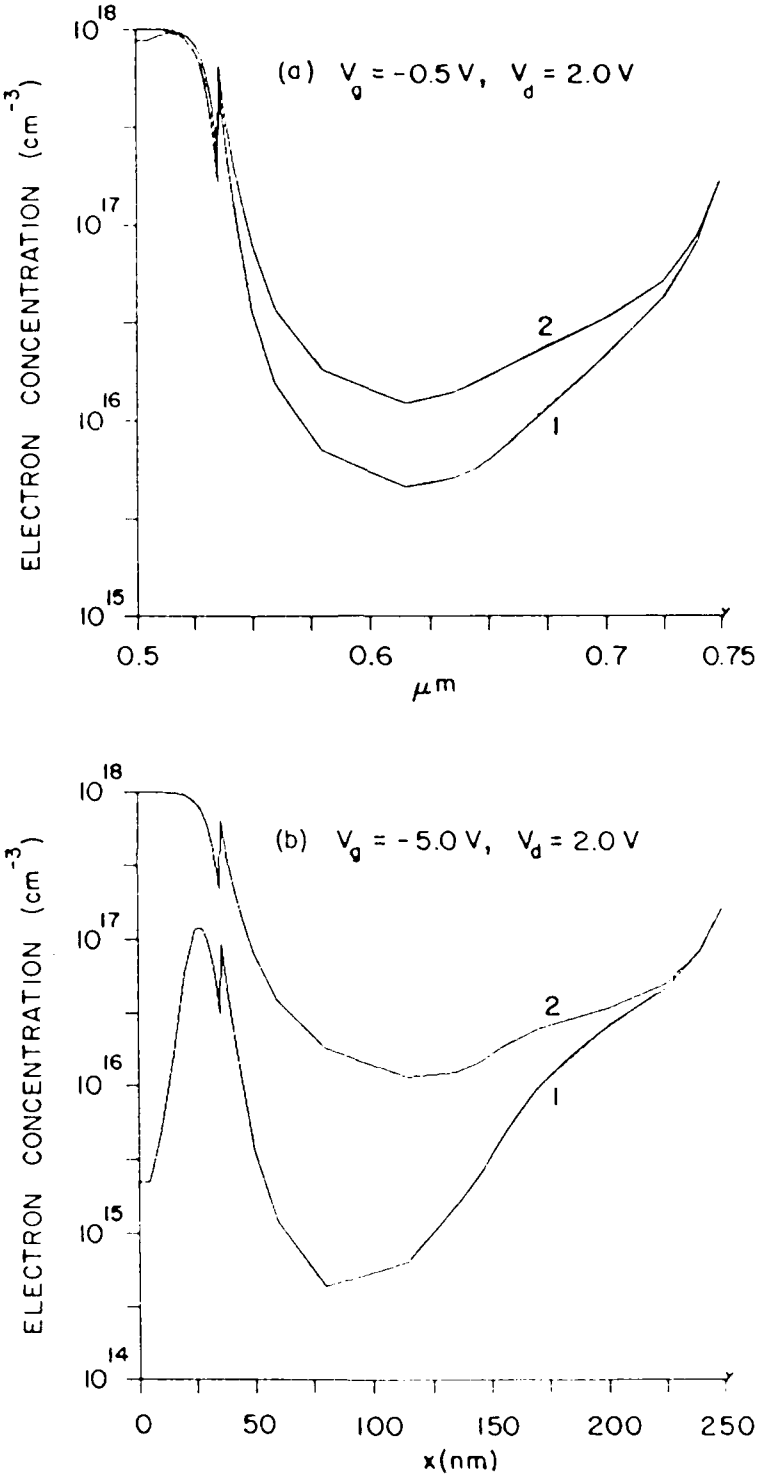


Figure 17. Variation of electron concentrations along the two lines denoted by (1) and (2) in Figure 3b for (a) V_G = -0.5 V, (b) V_G = -5.0 V.

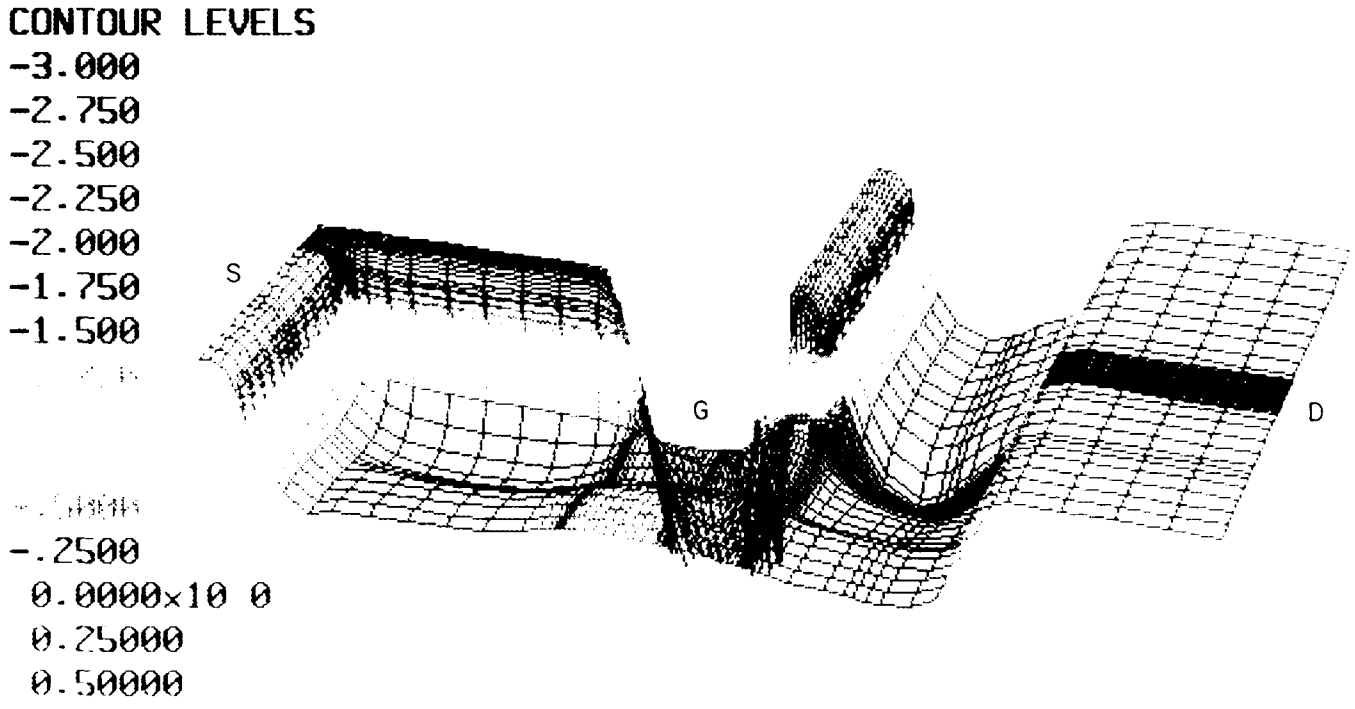


Figure 18. Three-dimensional plot of the electron concentration within the VHEMT for V_D = 2.0 V and V_G = 0.5 V.

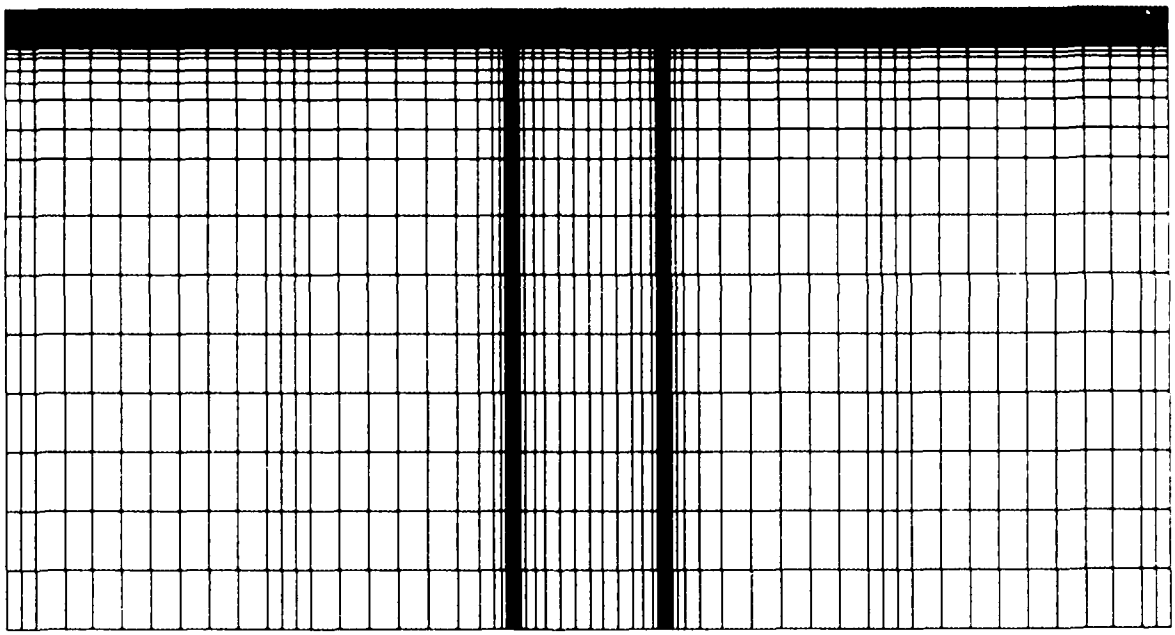


Figure 19. Grid structure used in the simulation of the PHEMT.

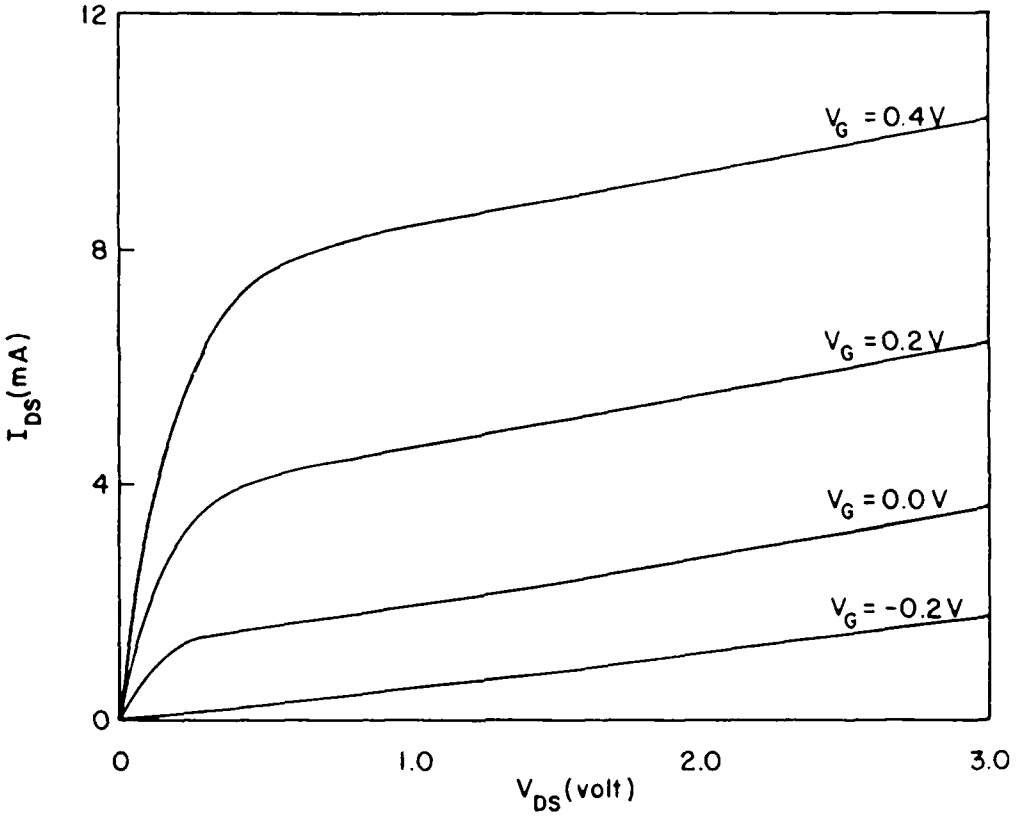


Figure 20a. The I-V characteristics of a 50 μm wide PHEMT.

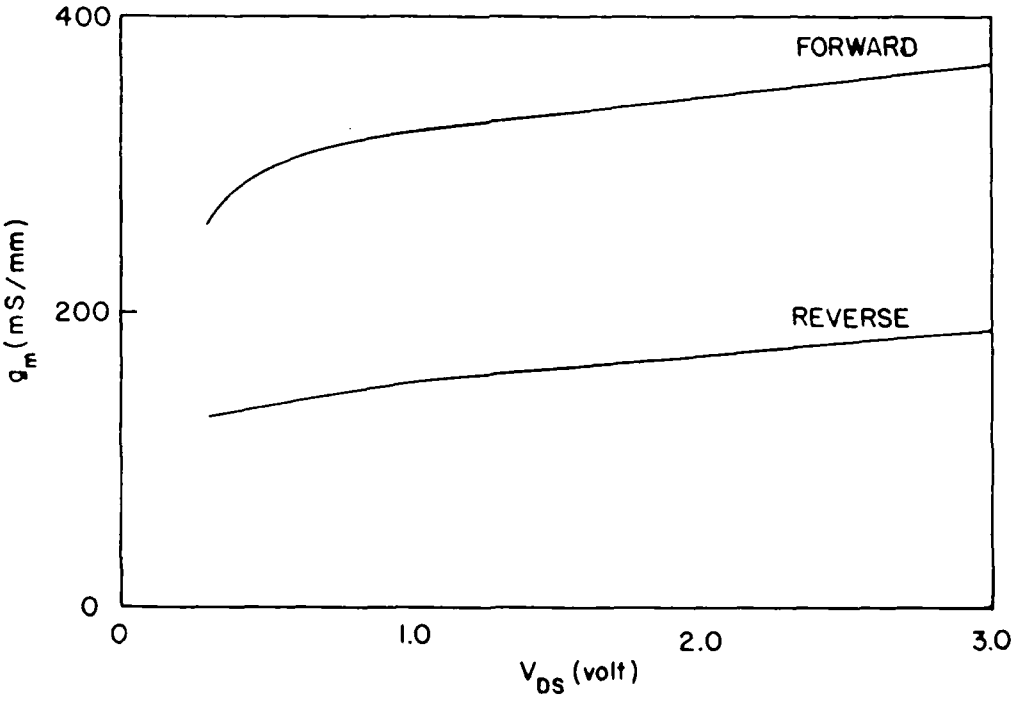


Figure 20b. Variation of the transconductance with Drain bias for the forward and reverse bias on the gate.

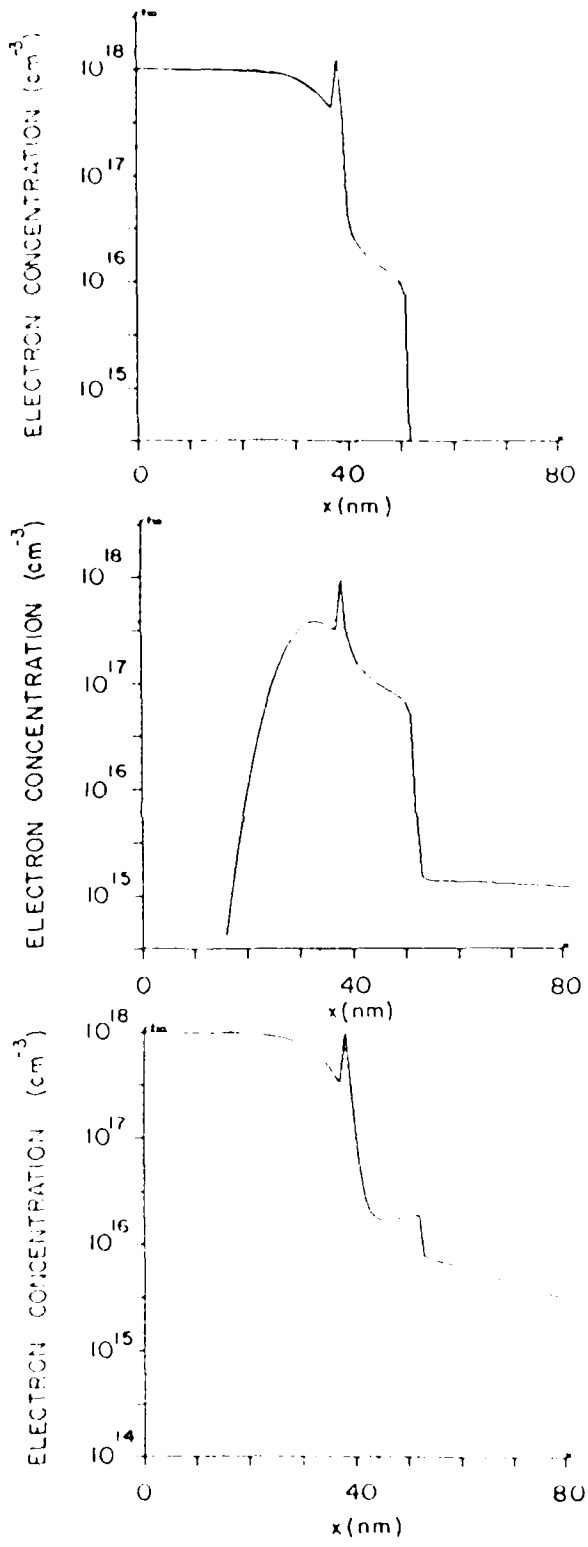


Figure 21. Variations of electron concentration in the PHEMT along lines normal to the center of (a) source (b) gate (c) drain for V_D = 1.0 V and V_G = 0.2 V.

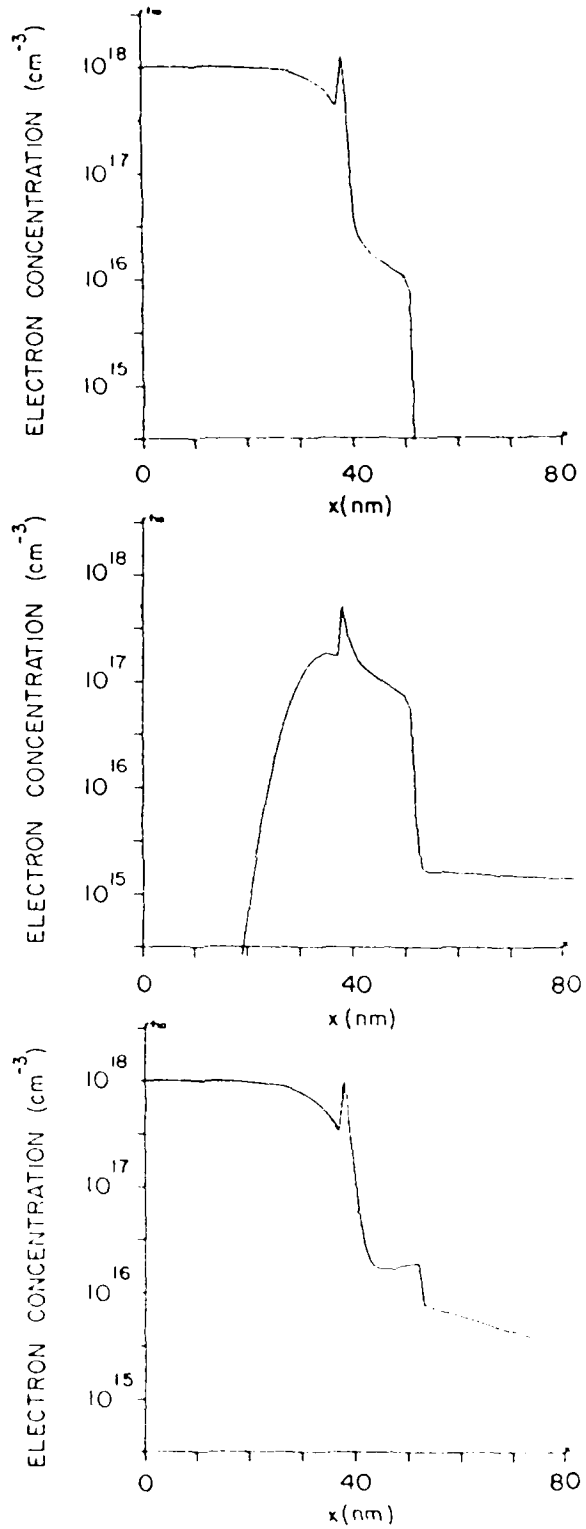


Figure 22. Variations of electron concentration in the PHEMT along lines normal to the center of (a) source (b) gate (c) drain for V_D = 1.0 V and V_G = 0.0 V.

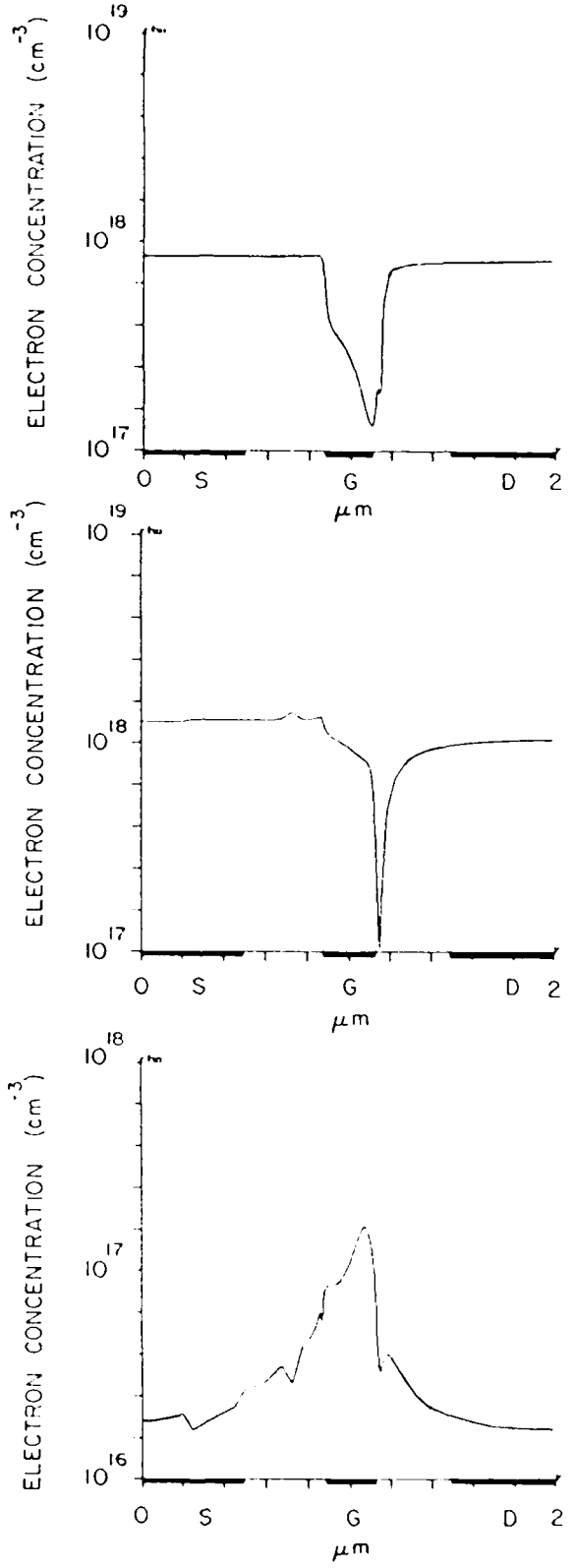


Figure 23. Variation of electron concentration in the PHEMT along lines parallel to the contacts and at a distance of (a) 10 nm, (b) 39 nm, (c) 45 nm from the contacts for V_D = 1.0 V and V_G = 0.2 V.

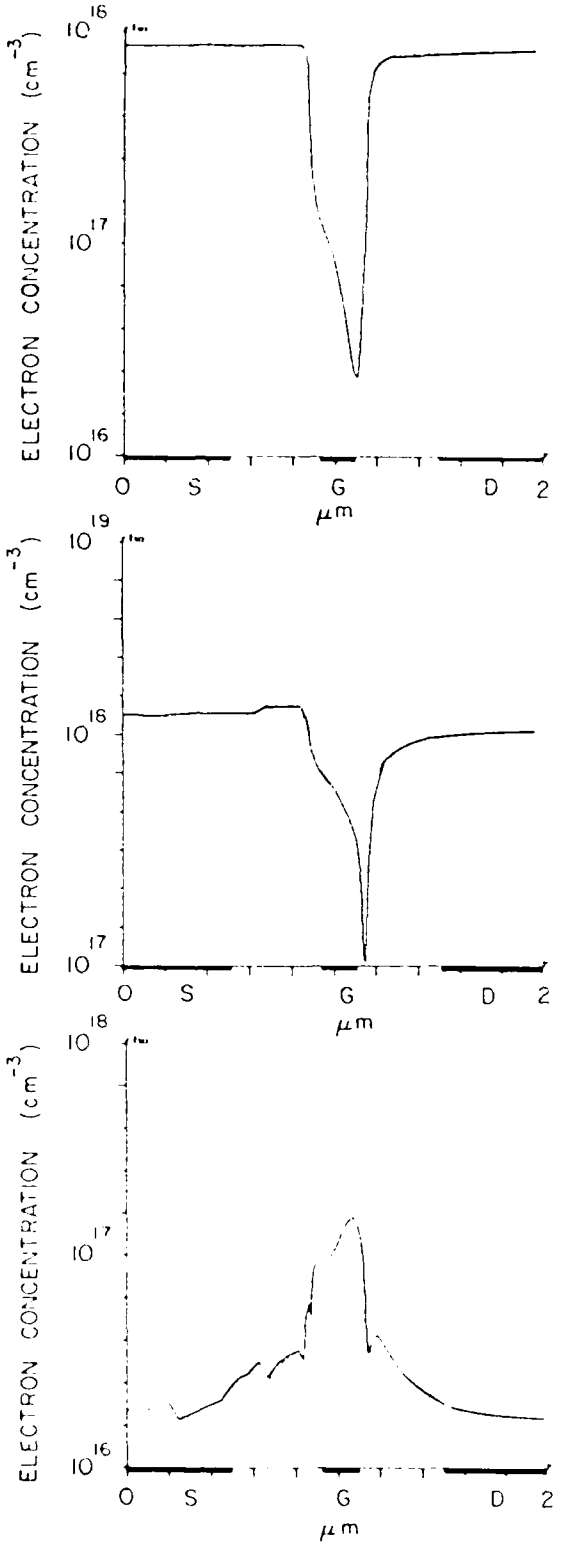


Figure 24. Variation of electron concentration in the PHEMT along lines parallel to the contacts and at a distance of (a) 10 nm, (b) 39 nm, (c) 45 nm from the contacts for V_D = 1.0 V and V_G = 0.0 V.

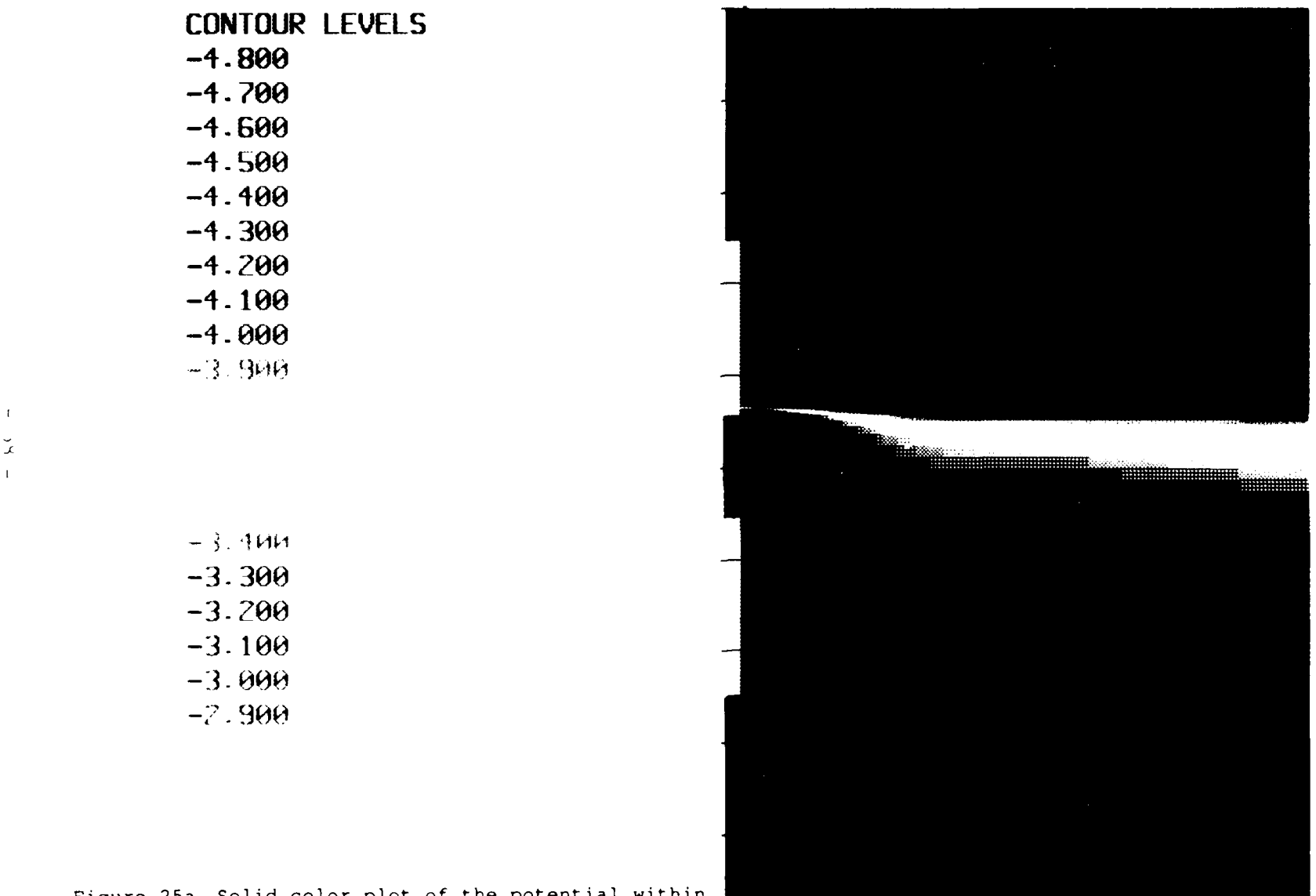


Figure 25a. Solid color plot of the potential within the PHEMT at V_D = 1.0 V and V_G = 0.2 V.

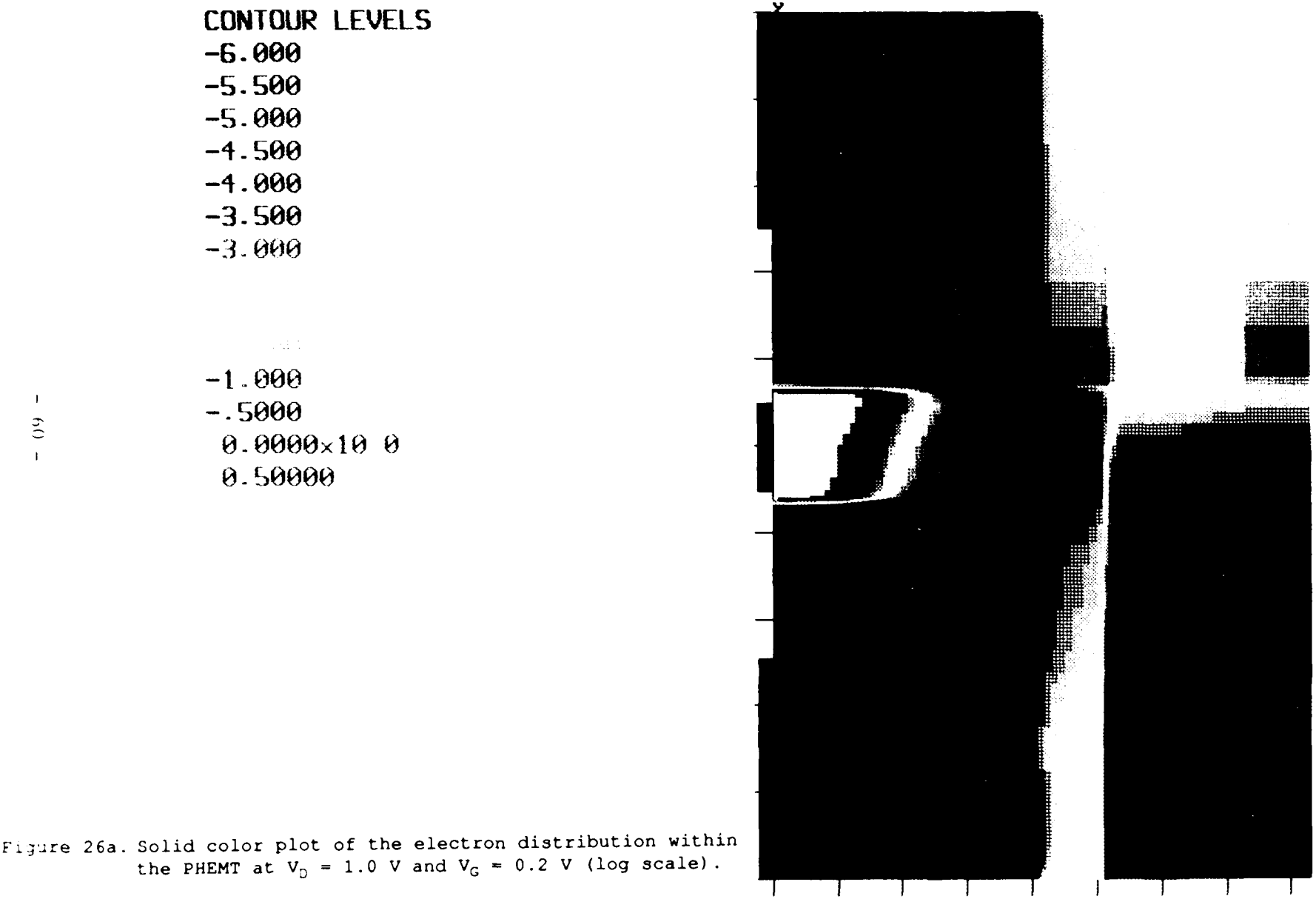


Figure 26a. Solid color plot of the electron distribution within the PHEMT at V_D = 1.0 V and V_G = 0.2 V (log scale).

CONTOUR LEVELS
-6.000
-5.500
-5.000
-4.500
-4.000
-3.500
-3.000

-1.000
-.5000
0.0000×10 0
0.50000

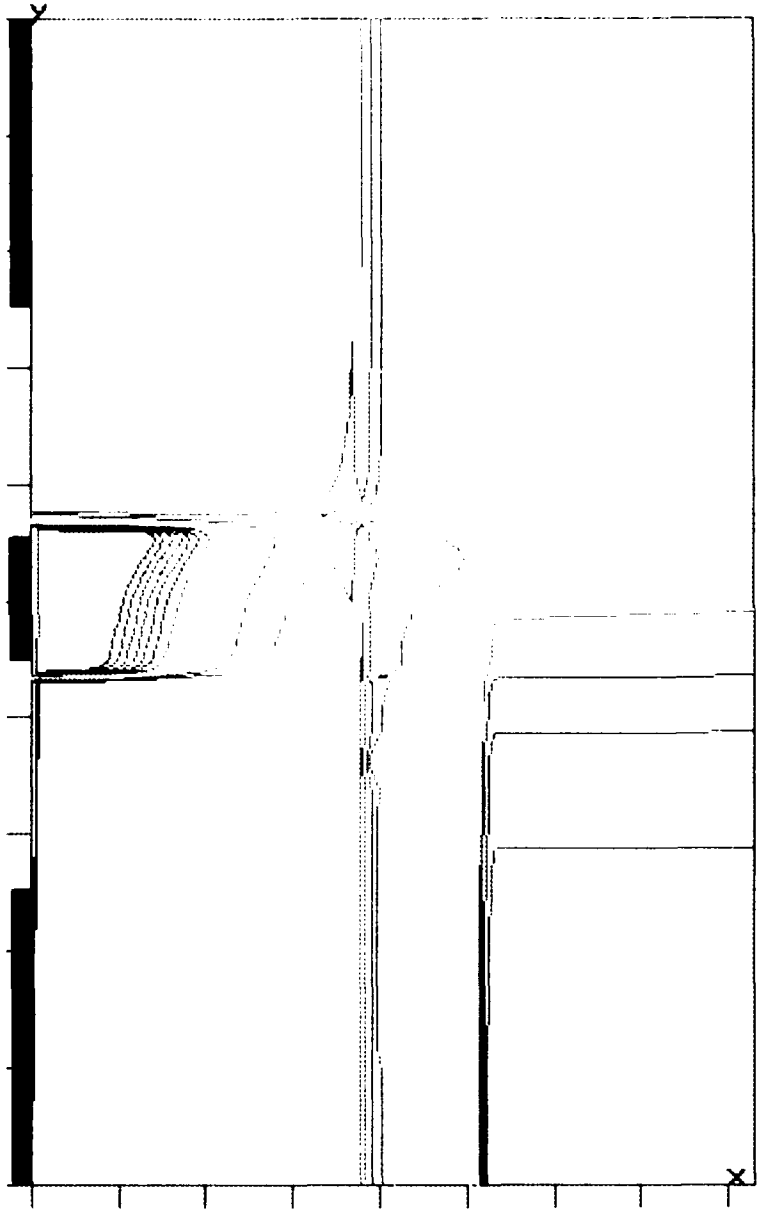


Figure 26b. Color contour plot of the equal electron density lines within the PHEMT (log scale).

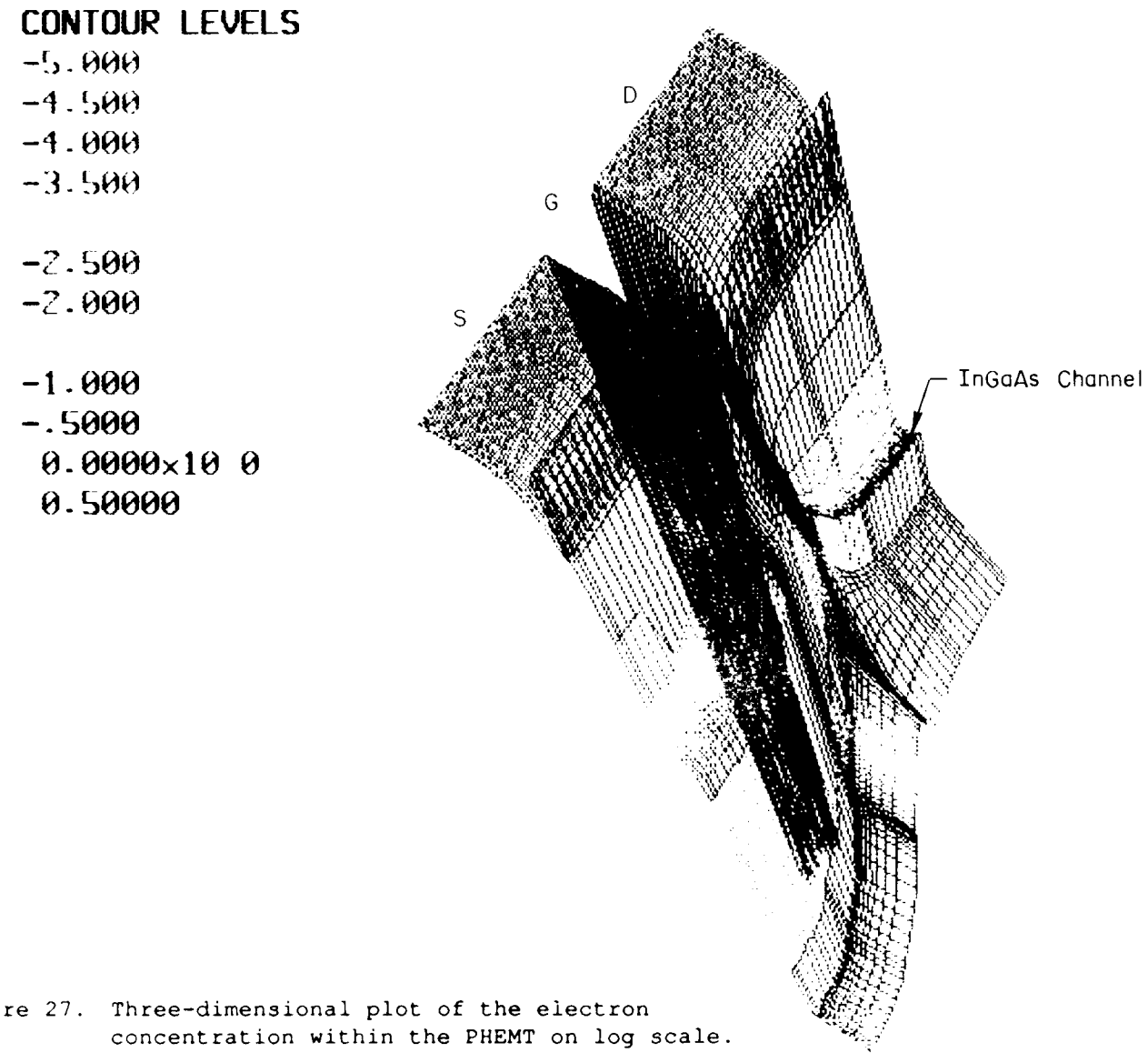


Figure 27. Three-dimensional plot of the electron concentration within the PHEMT on log scale.

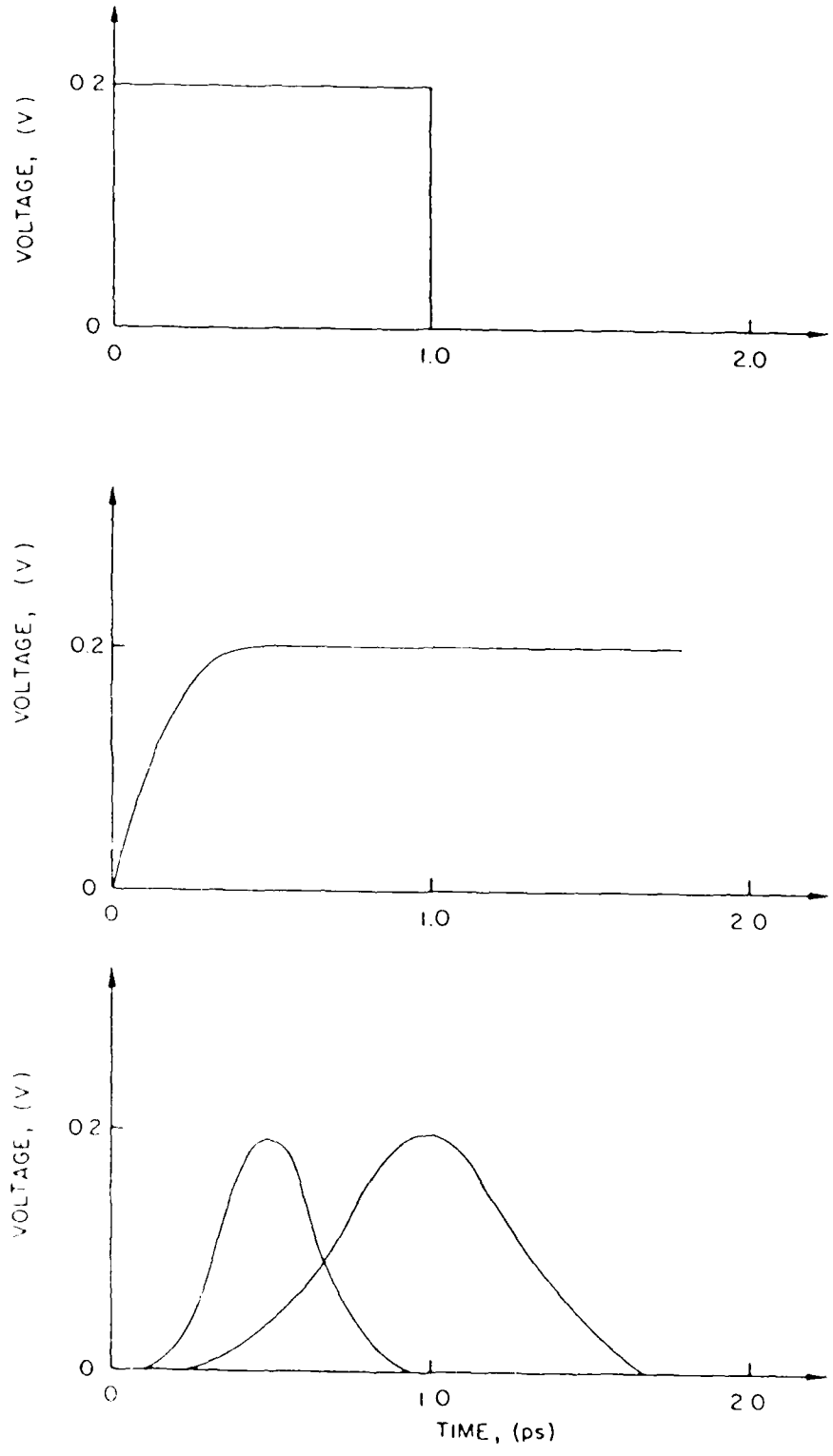
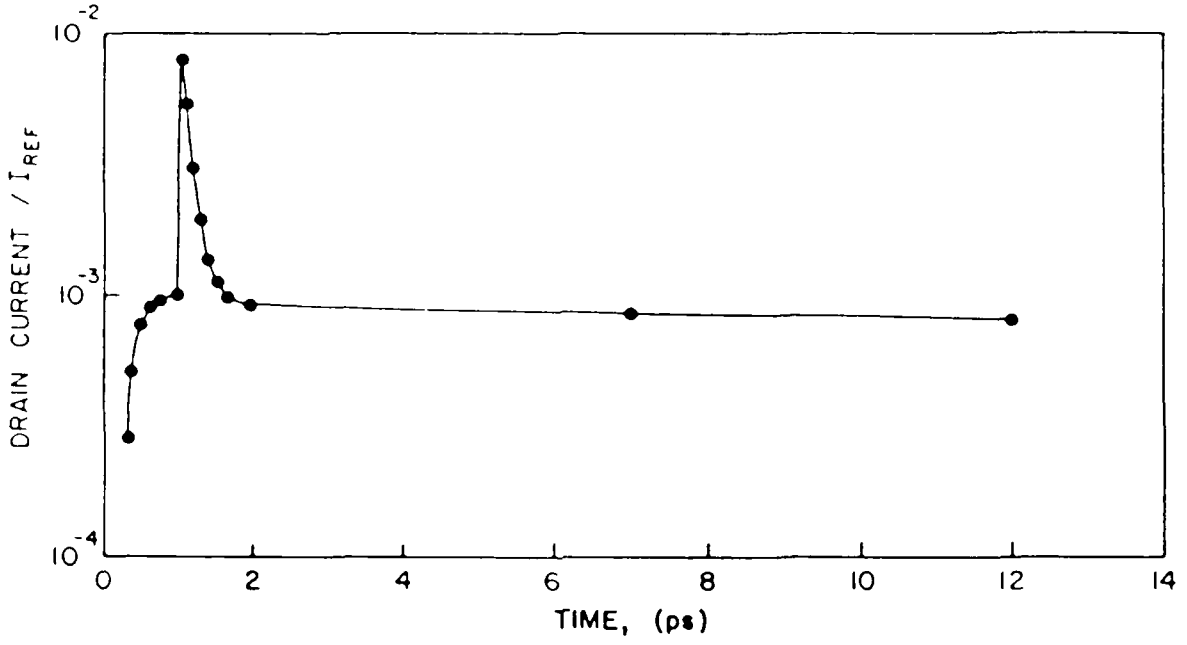


Figure 28. The shapes of voltage pulses used in perturbing the gate of the PHEMT.



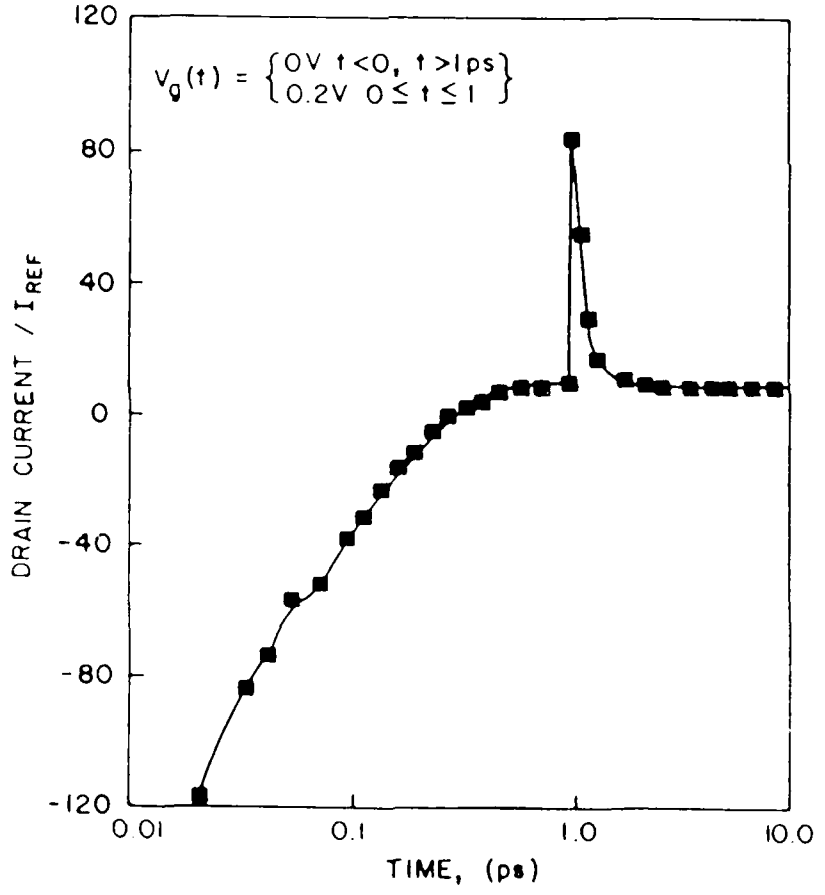


Figure 29. Transient drain response of the PHEMT after being perturbed by the voltage pulse in Figure 28a (a) linear scale (b) log scale.

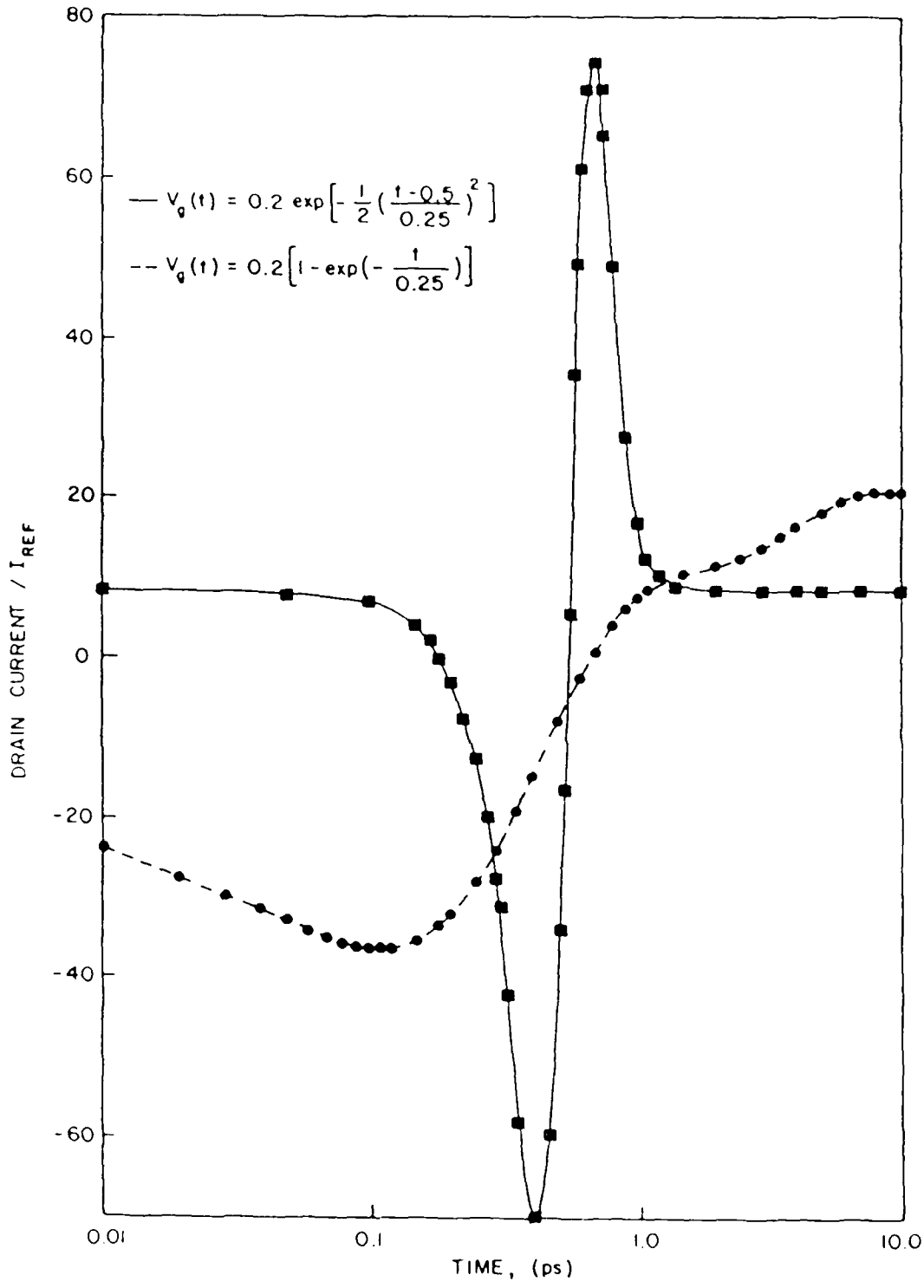


Figure 30. Transient response of the PHEMT to the pulses shown in Figure 28a and 28b.

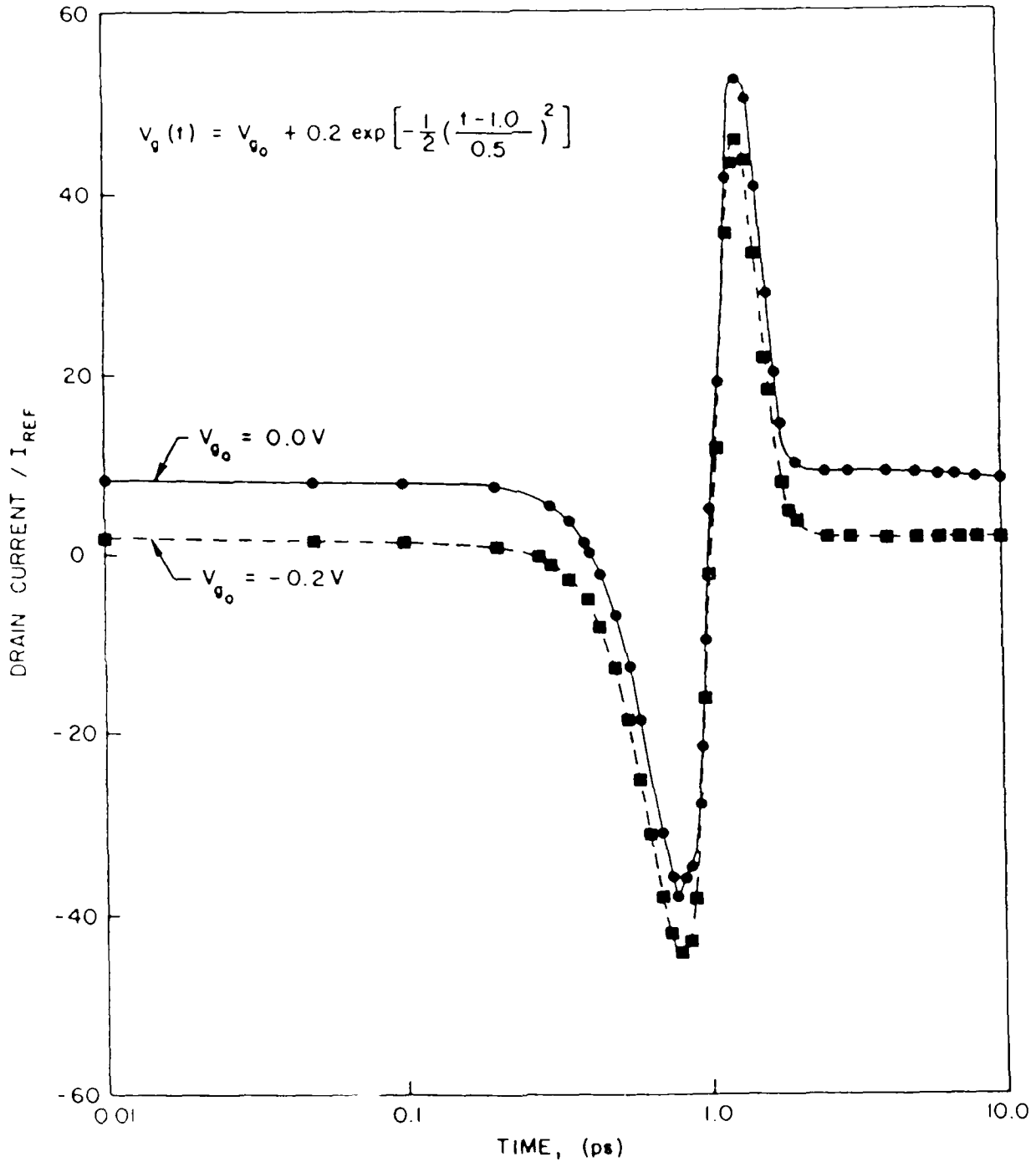


Figure 31. Transient response of the PHEMT to a Gaussian pulse for gate biases (1) -0.2 V, (2) 0.0 V.

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